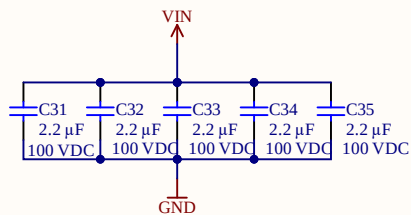
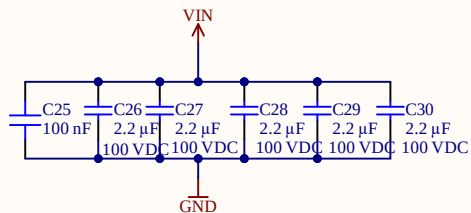
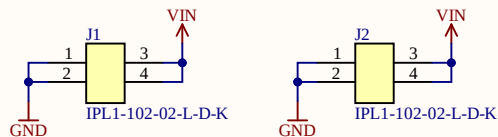
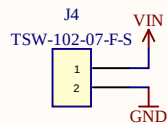


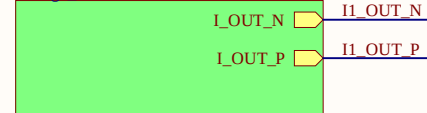
VIN -> 7V to 65V



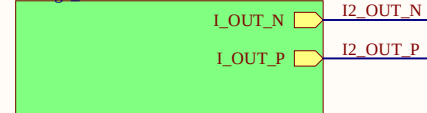
Alternative



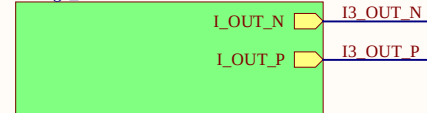
Measurement_1
Voltage_Measurement.SchDoc



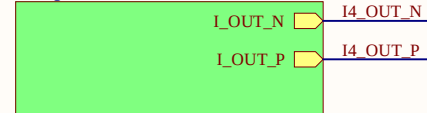
Measurement_2
Voltage_Measurement.SchDoc



Measurement_3
Voltage_Measurement.SchDoc



Measurement_4
Voltage_Measurement.SchDoc



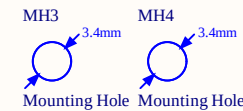
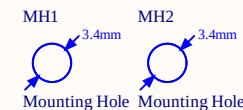
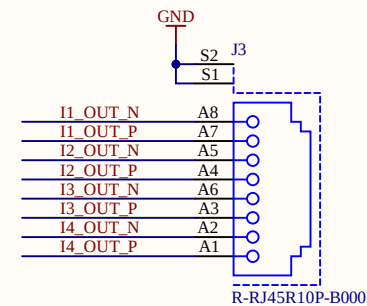
power_supply
Power_Supply.SchDoc



Serial1
Serial
Serialnumber 6.3 x 6.3 mm

INFO1
Project
ProjectRevision
AuthorParam
ProjectDate
Design Information

LOGO1
UZ Logo
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$$R_{FBT}[k\Omega] = R_{FBB}[k\Omega] \times \left(\frac{V_{OUT}[V]}{1V} - 1 \right)$$

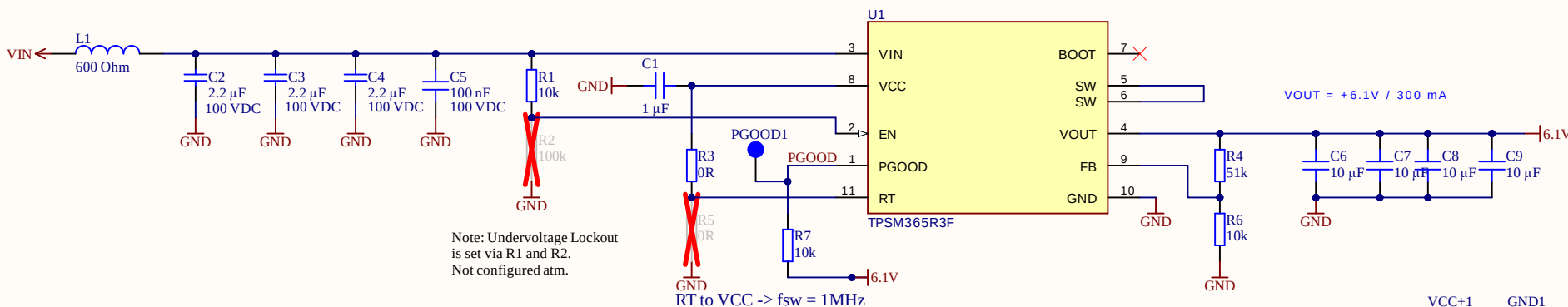
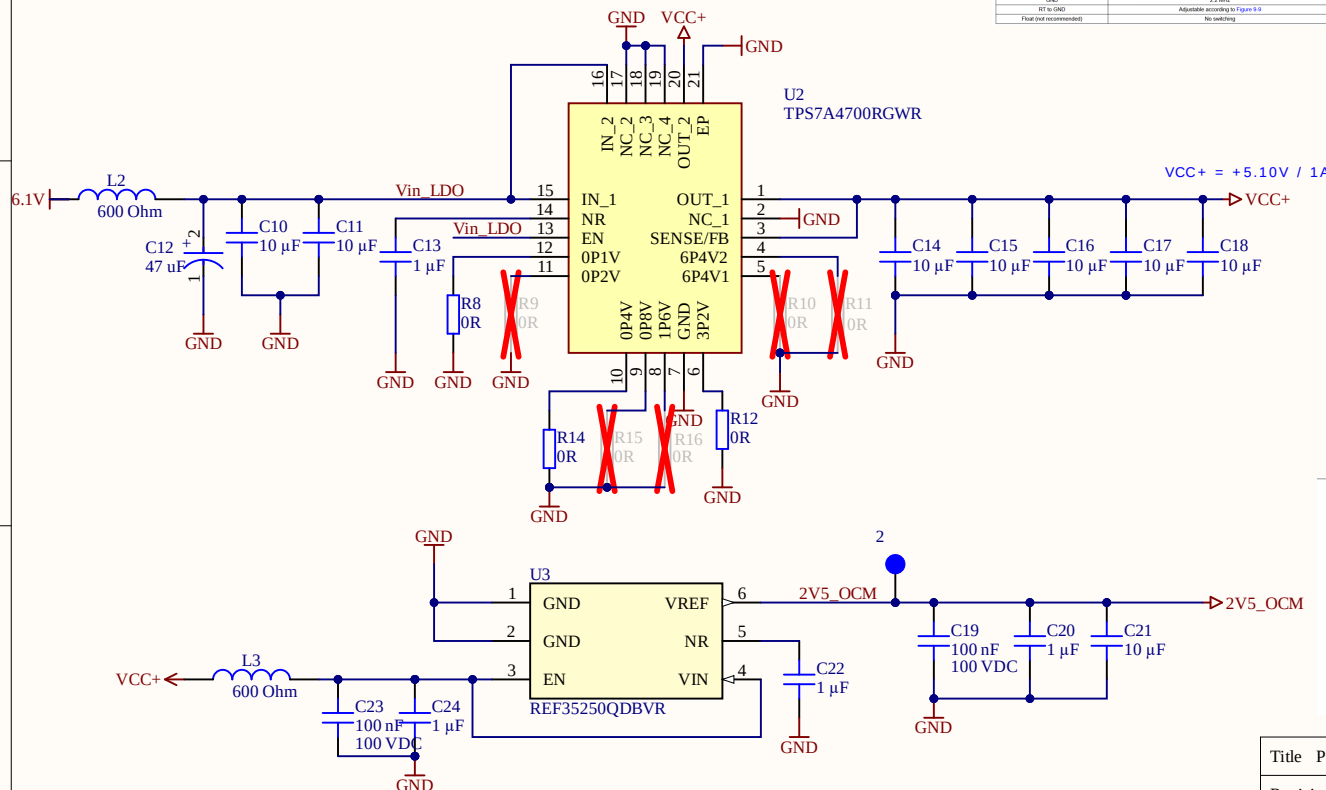
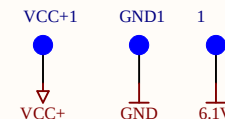


Table 9-5. RT Pin Setting	
RT INPUT	SWITCHING FREQUENCY
VCC	1 MHz
GND	2.2 MHz
RT to GND	Adjustable according to Figure 9-8
Foot (not recommended)	No switching



7.5.1 ANY-OUT Programmable Output Voltage

Both devices can be used in ANY-OUT mode. For ANY-OUT operation, the TPS7A4700 and TPS7A4701 do not use external resistors to set the output voltage, but use device pins 4, 5, 6, 8, 9, 10, 11, and 12 to program the regulated output voltage. Each pin is either connected to ground (active) or is left open (floating). The ANY-OUT programming is set by Equation 2 as the sum of the internal reference voltage ($V_{REF} = 1.4V$) plus the accumulated sum of the respective voltages assigned to each active pin; that is, 100 mV (pin 12), 200 mV (pin 11), 400 mV (pin 10), 800 mV (pin 9), 1.6 V (pin 8), 3.2 V (pin 6), 6.4 V (pin 5), or 6.4 V (pin 4). Table 1 summarizes these voltage values associated with each active pin setting for reference. By leaving all program pins open, or floating, the output is thereby programmed to the minimum possible output voltage equal to V_{REF} .

Table 1. ANY-OUT Programmable Output Voltage	
ANY-OUT PROGRAMMING (Active Low)	ADDITIVE OUTPUT VOLTAGE LEVEL
Pin 4 (BP4V2)	6.4 V
Pin 5 (BP4V1)	6.4 V
Pin 6 (BP2)	3.2 V
Pin 8 (BP8)	1.6 V
Pin 9 (BP8)	800 mV
Pin 10 (BP4)	400 mV
Pin 11 (BP2)	200 mV
Pin 12 (BP1)	100 mV

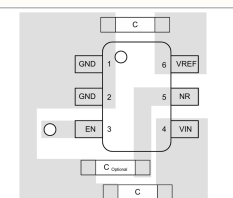
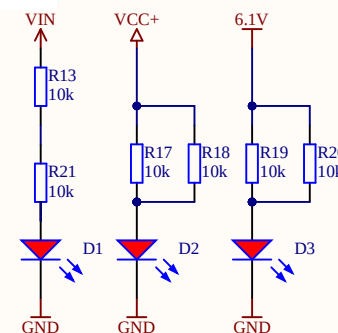


Figure 10-4. Layout Example



NR -> Noise reduction cap

Title Power_Supply.SchDoc
Revision: Rev01 Design Engineer: Nina Diringer
Project: uz_per_voltage_measurement.PjPcb

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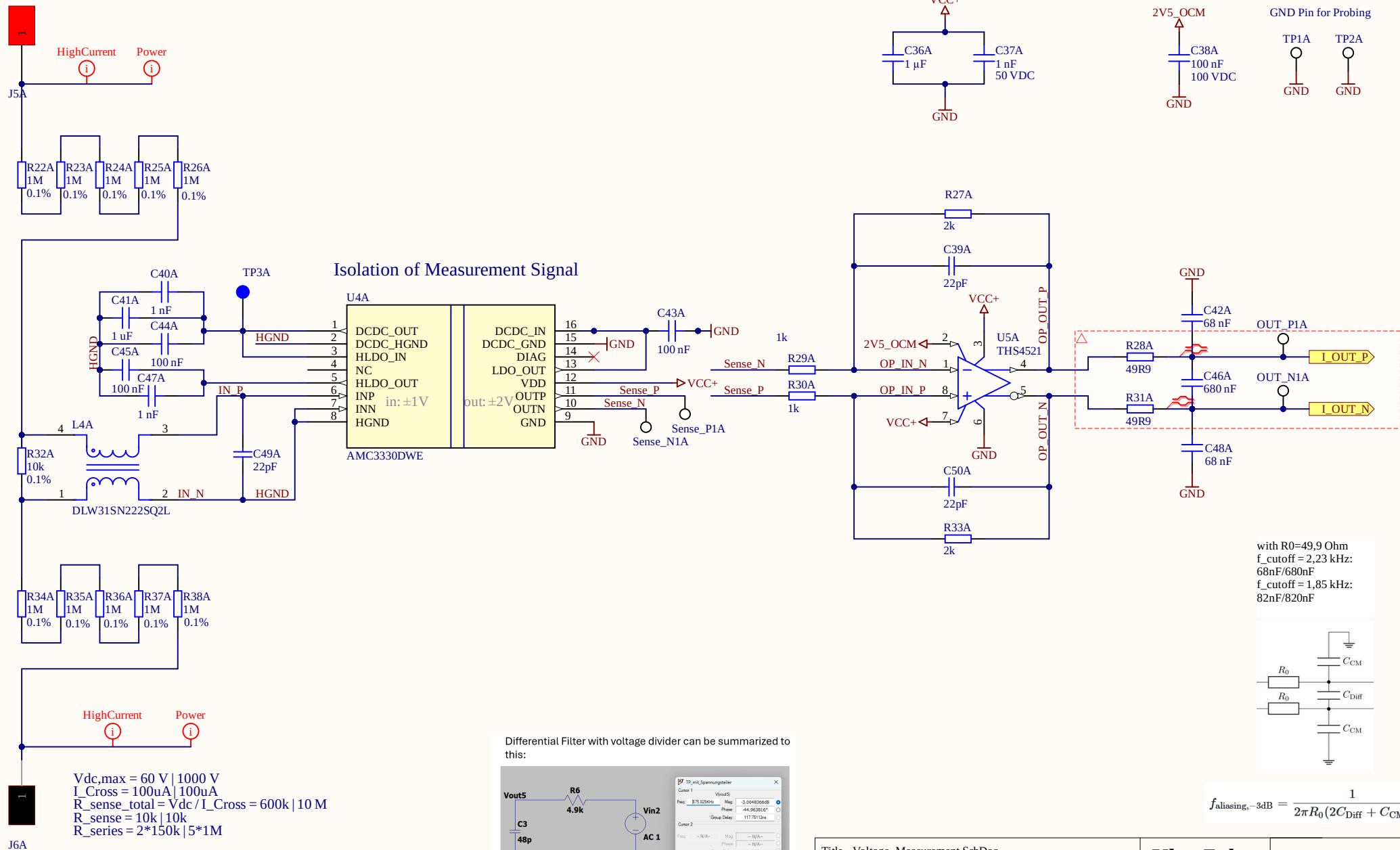
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4



Title Voltage_Measurement.SchDoc

Revision: Rev01

Design Engineer: Nina Diringer

Project: uz_per_voltage_measurement.PjPcb

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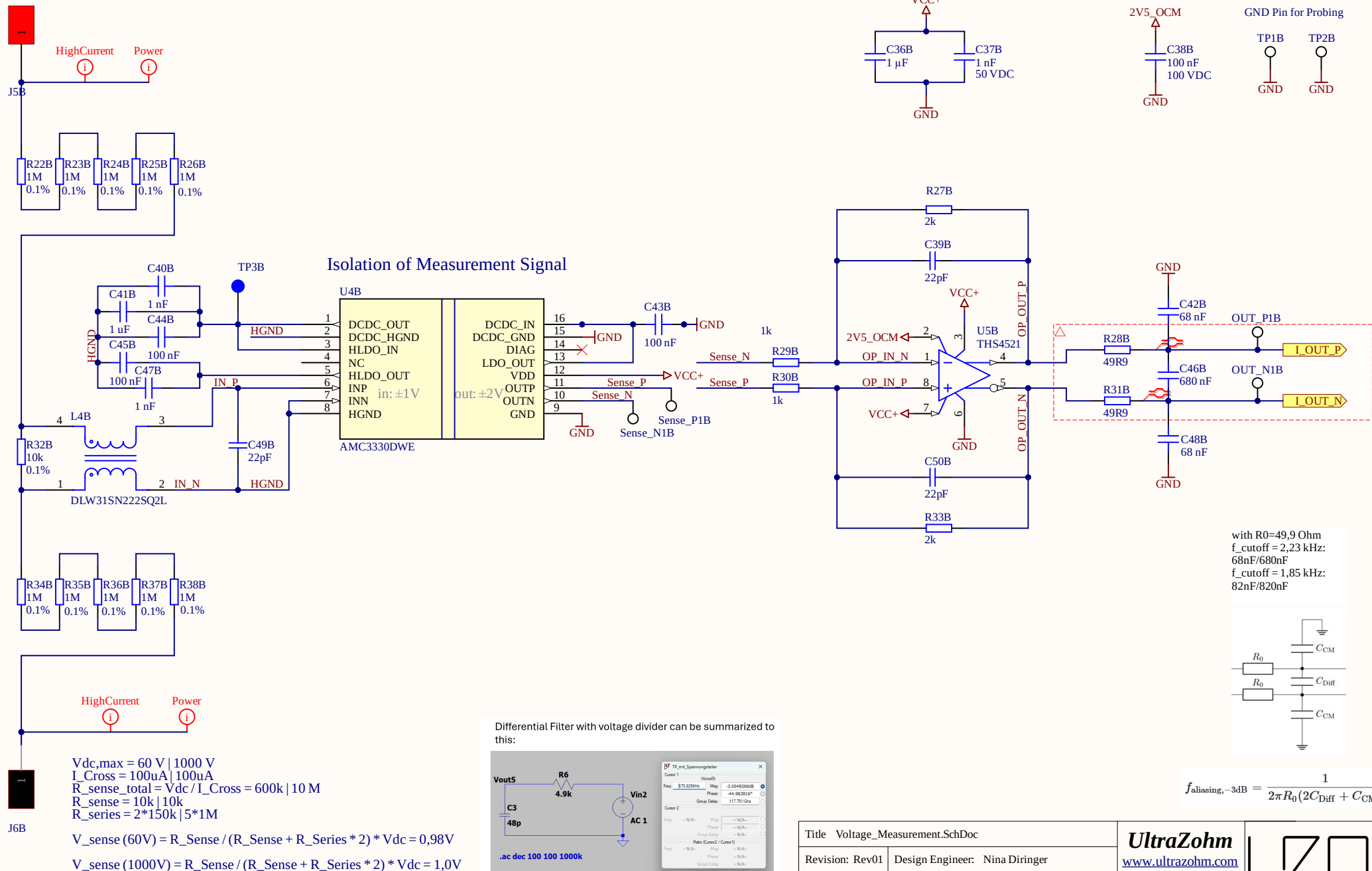


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$$f_{\text{aliasing}, -3\text{dB}} = \frac{1}{2\pi R_0 (2C_{\text{Diff}} + C_{\text{CM}})}$$

Title Voltage_Measurement.SchDoc

Revision: Rev01

Design Engineer: Nina Diringer

Project: uz_per_voltage_measurement.PjPcb

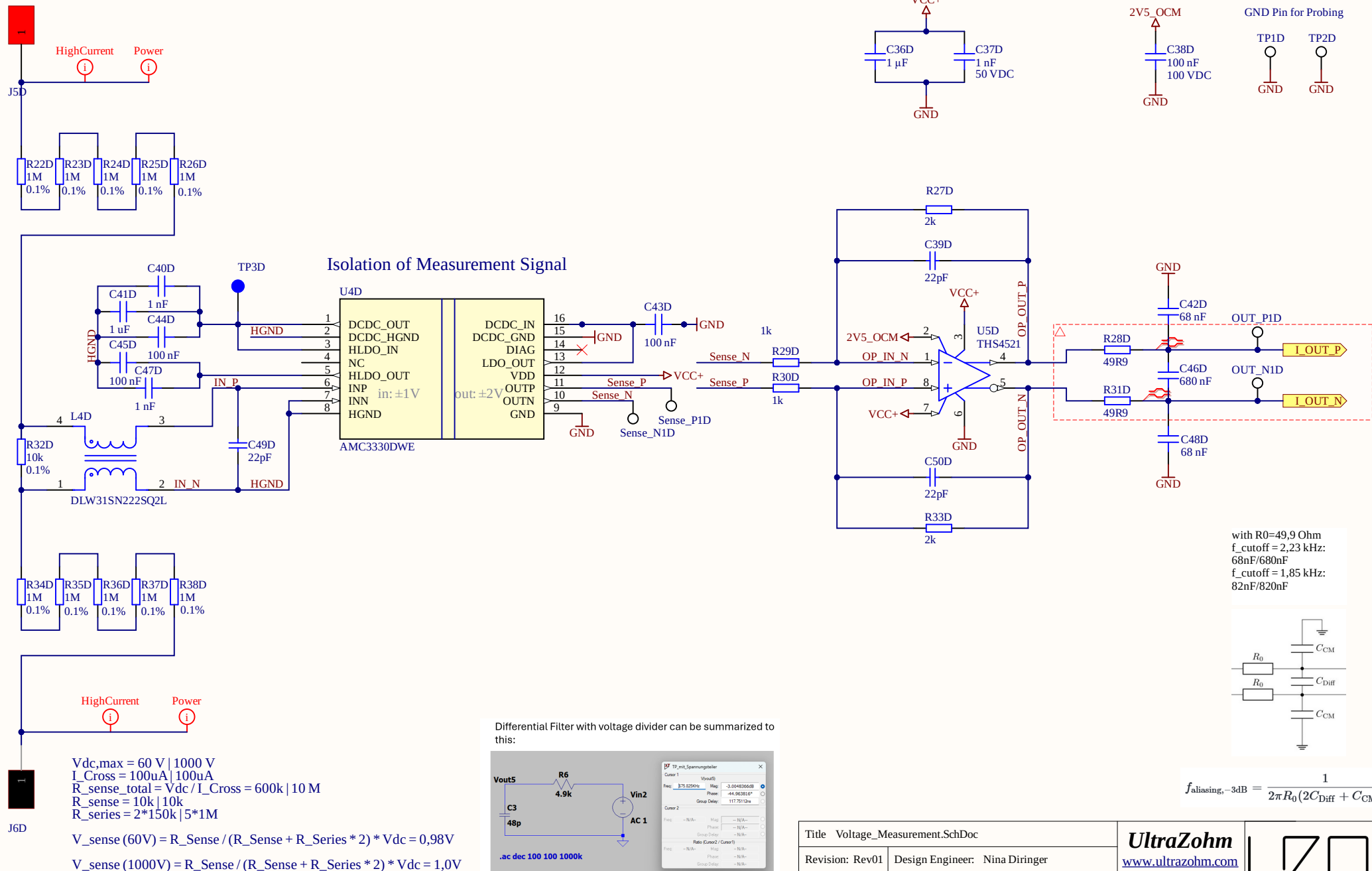
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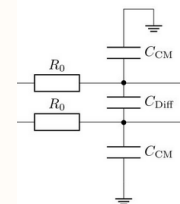
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Sheet 3 of 3





$$f_{\text{aliasing}, -3\text{dB}} = \frac{1}{2\pi R_0 (2C_{\text{Diff}} + C_{\text{CM}})}$$



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