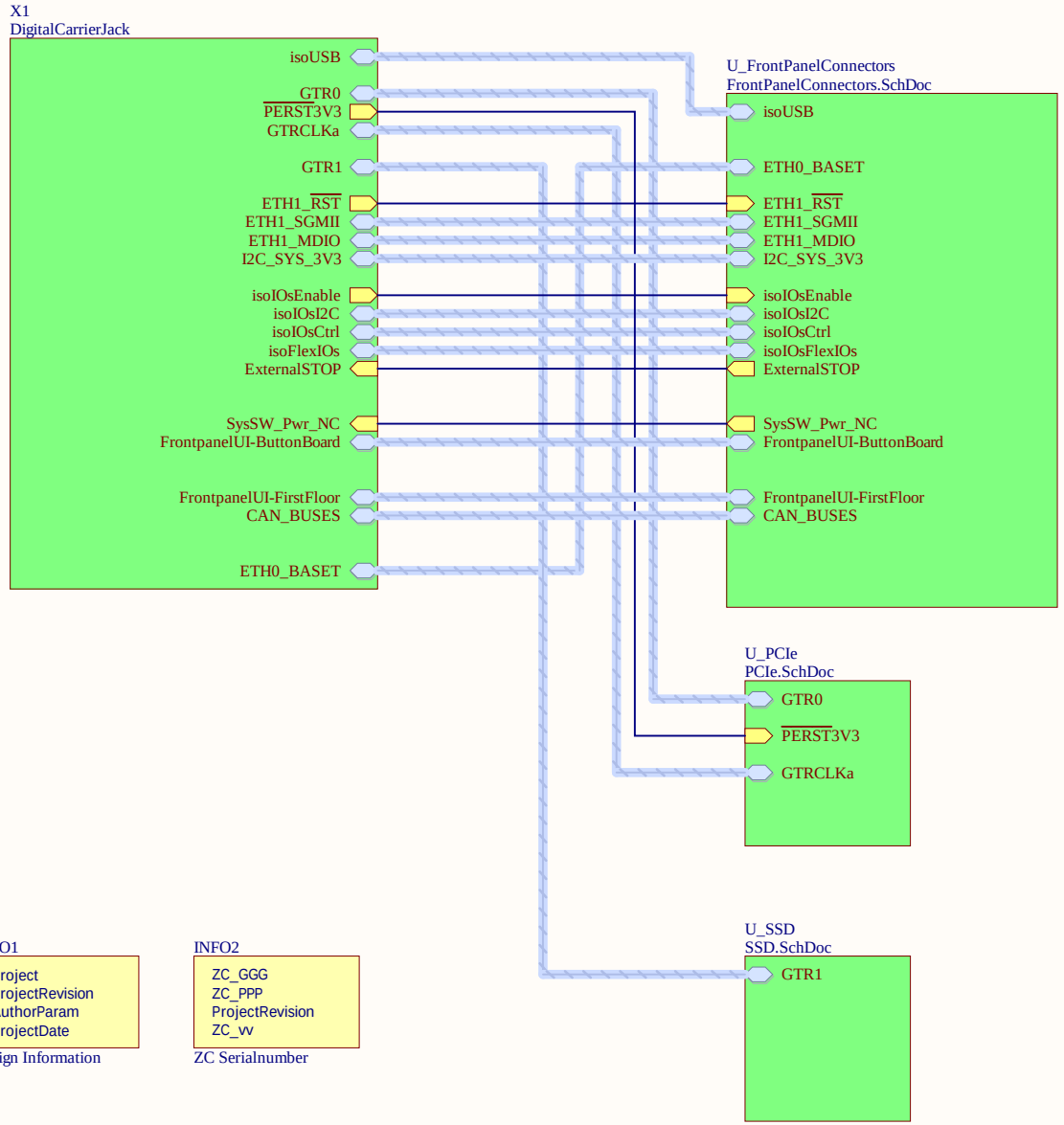


Choose size of UZ logo by choosing footprint...

LOGO1

INFO1

Project
ProjectRevision
AuthorParam
ProjectDate

Design Information

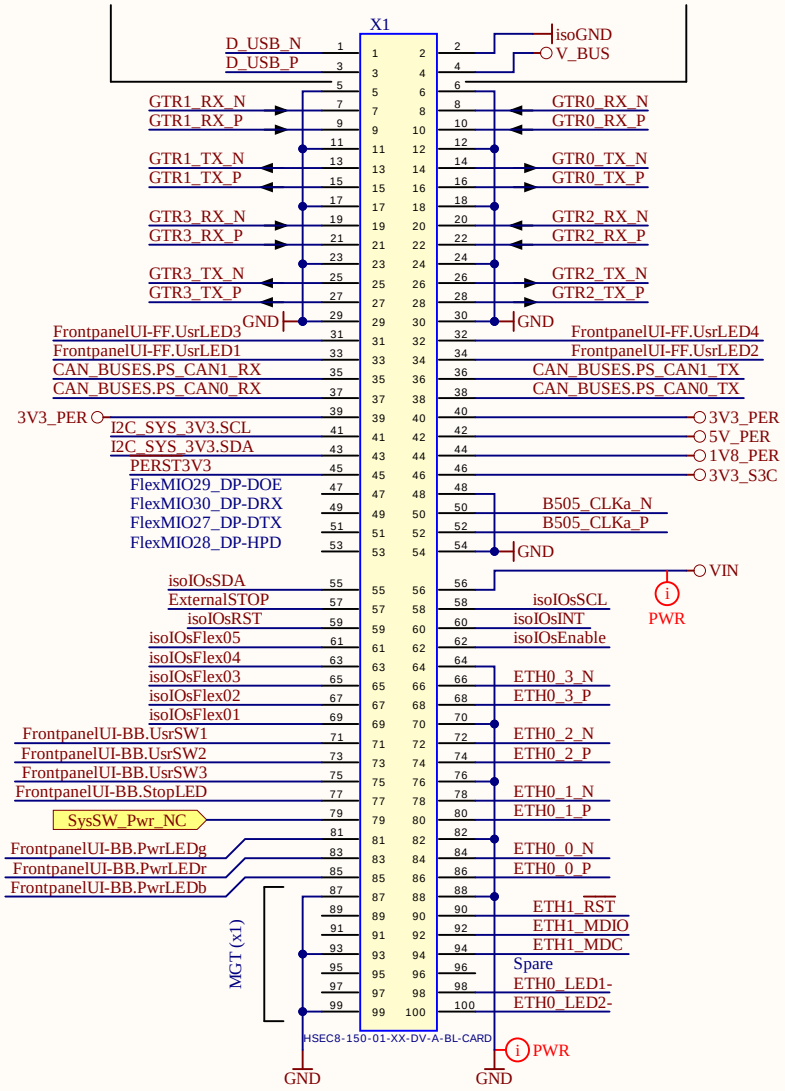
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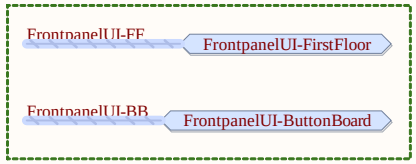
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ZC_PPP
ProjectRevision
ZC_vv

ZC Serialnumber

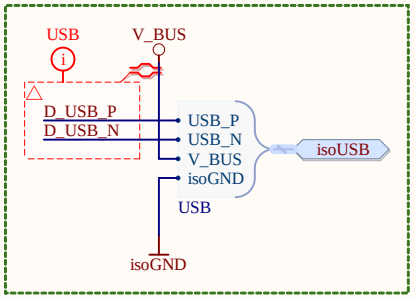
Title TopSheet.SchDoc		**UltraZohm**	
Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 1 of 36	

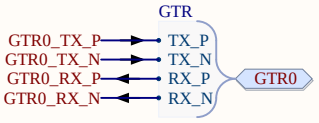
NB: VIN is always active - i.e., even if the system is (soft-)switched off

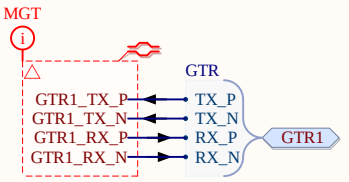


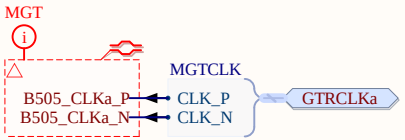


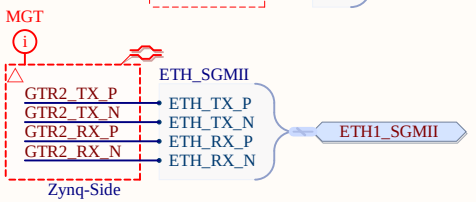
Currently not (yet?) instantiated function groups:
- DP option
- Anything else that one could implement using the 4 (S³C-connected) FlexMIOs 27 to 30 and/or I²C0 :-)

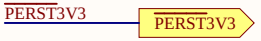


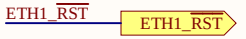


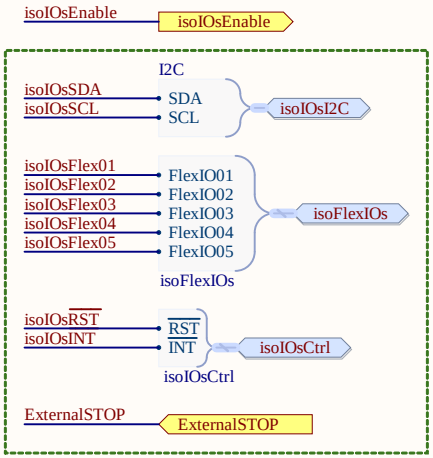




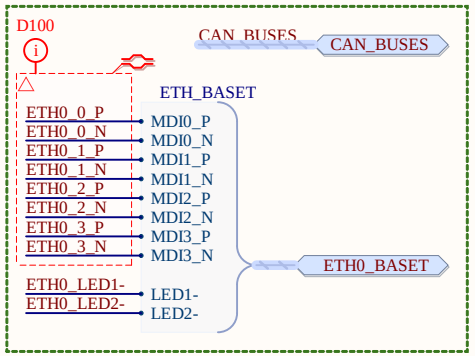






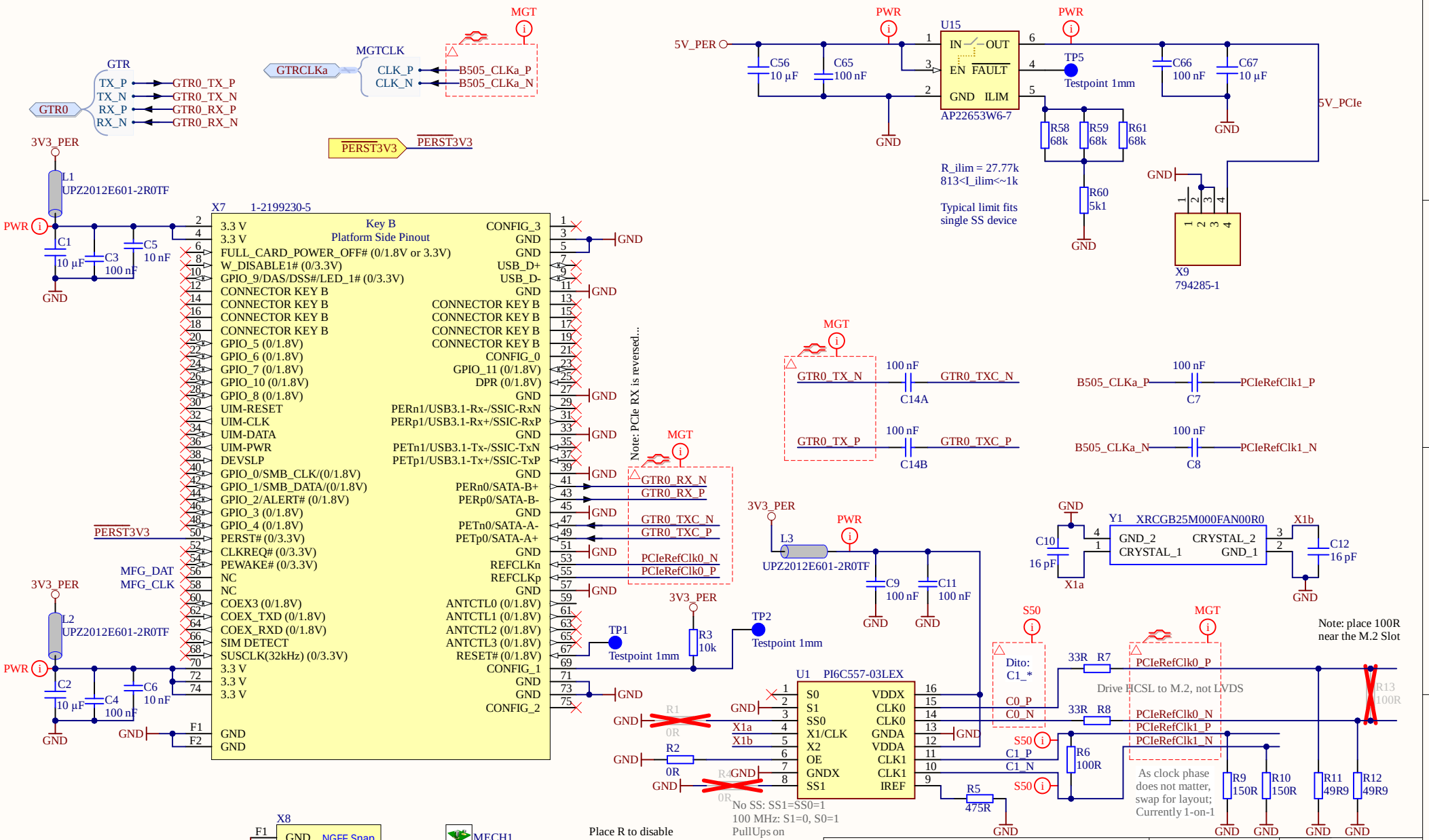




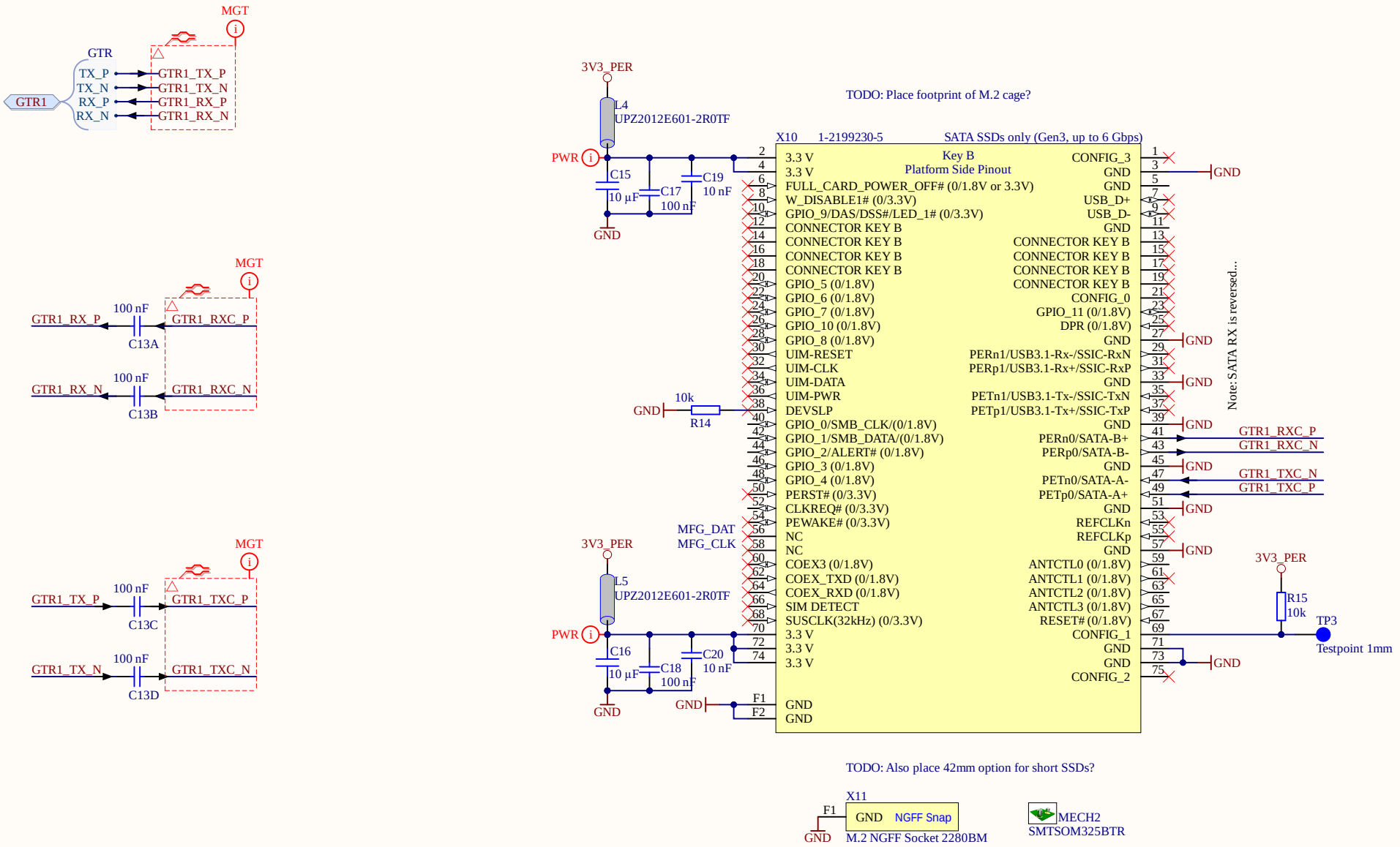




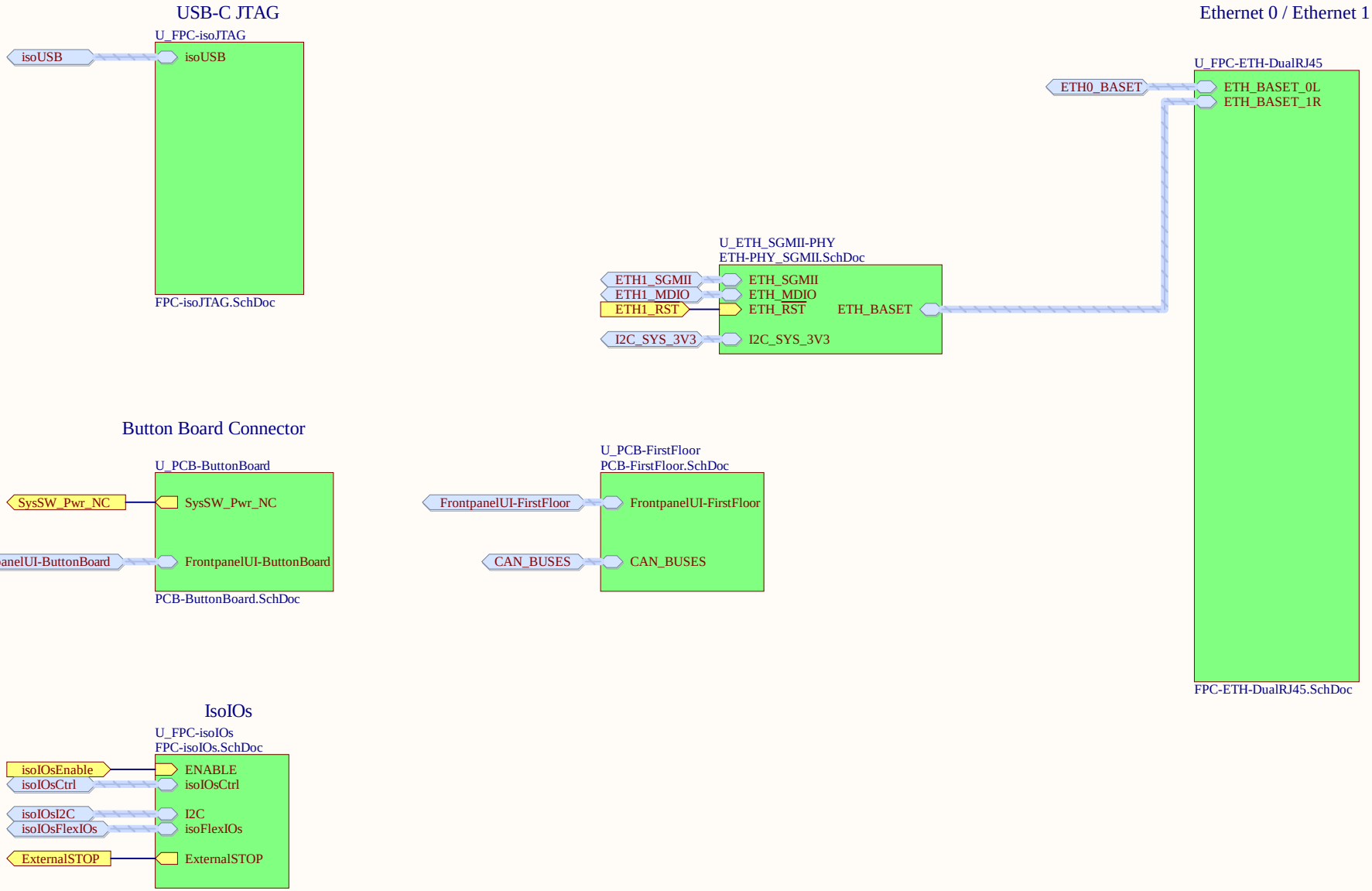
Title DigitalCarrierJack.SchDoc		UltraZohm www.ultrazohm.com
Revision: 03	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026 Sheet 2 of 36



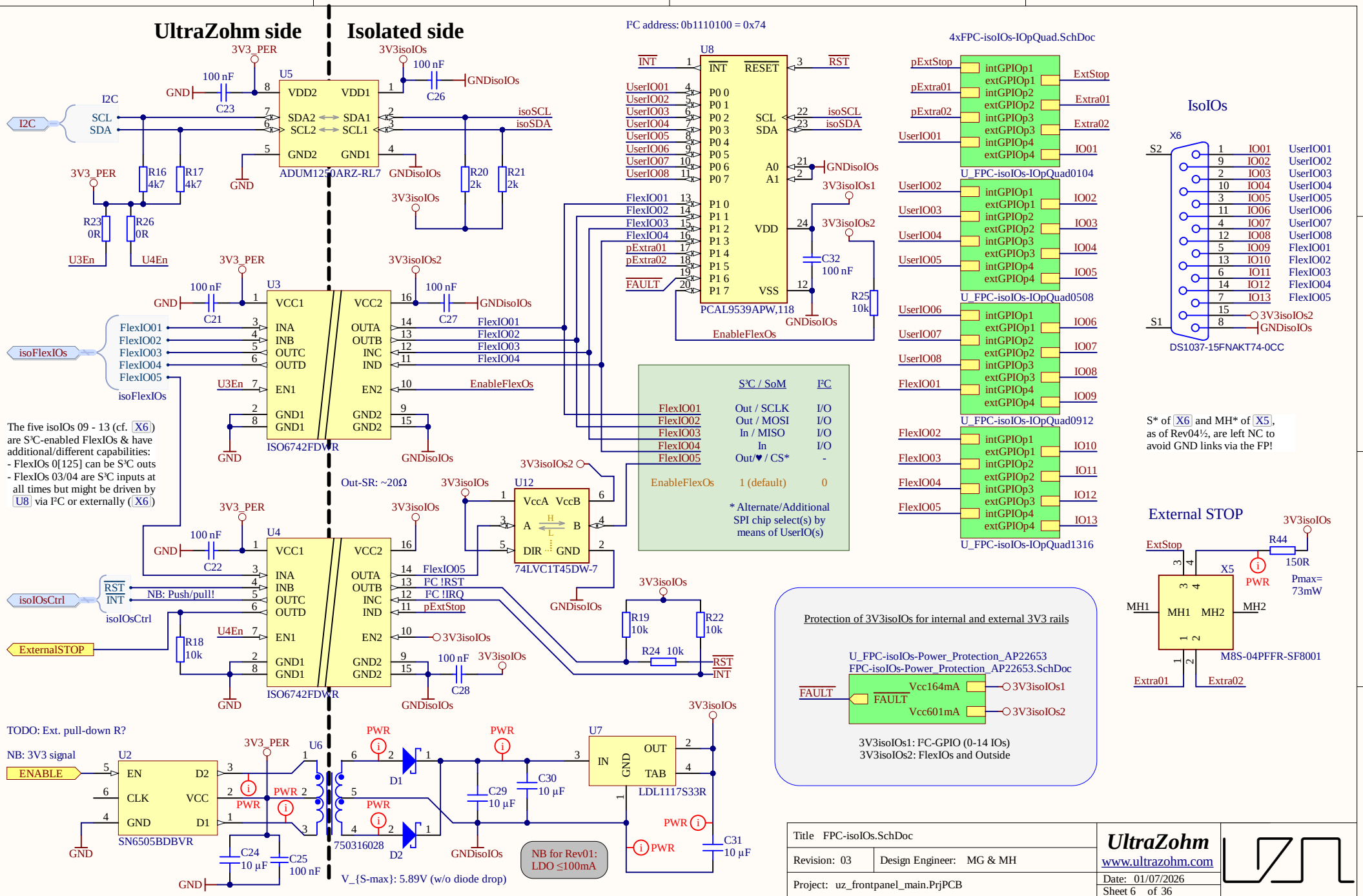
Title PCIe.SchDoc		UltraZohm
Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026
		Sheet 3 of 36

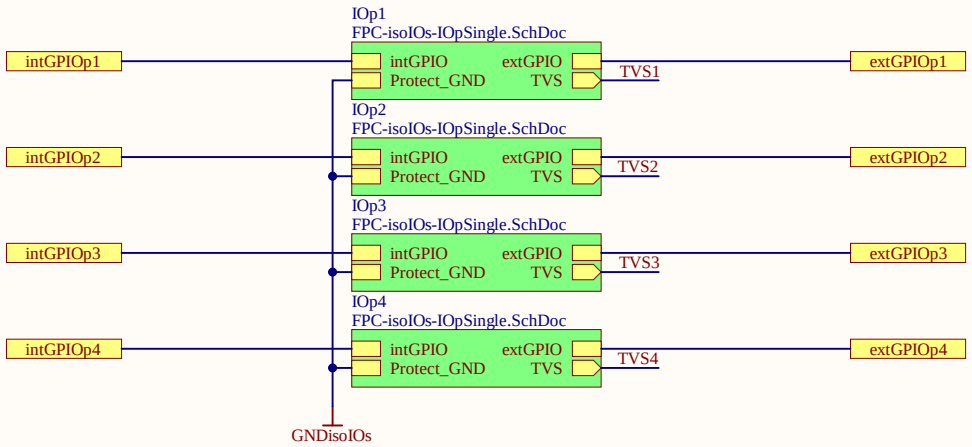


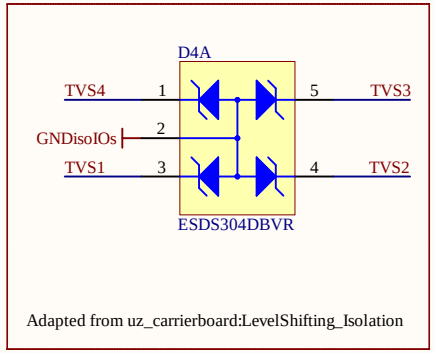
Title SSD.SchDoc		**UltraZohm**	
Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 4 of 36	



Title FrontPanelConnectors.SchDoc		UltraZohm	
Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 5 of 36	

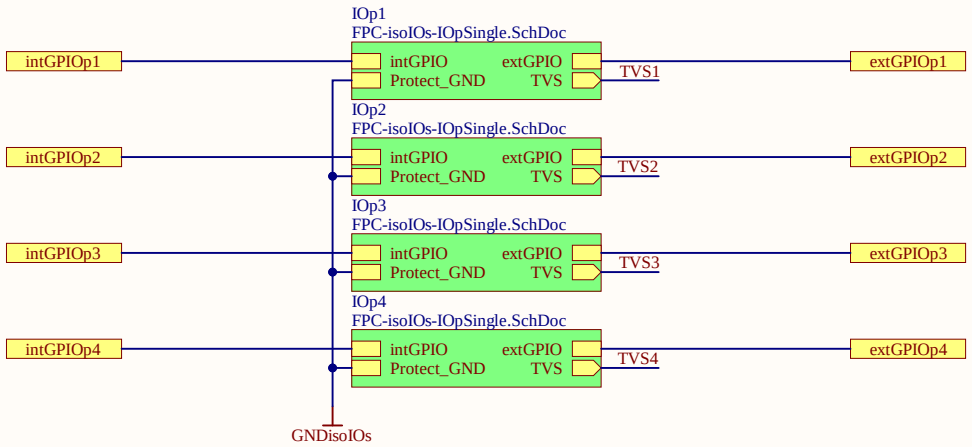

UltraZohm side
Isolated side
I²C address: 0b1110100 = 0x74
4xFPC-isoIOs-IOpQuad.SchDoc
IsoIOs
The five isoIOs 09 - 13 (cf. X6) are S³C-enabled FlexIOs & have additional/different capabilities:
- FlexIOs 0[125] can be S³C outs
- FlexIOs 03/04 are S³C inputs at all times but might be driven by U8 via I²C or externally (X6)
S³C / SoM
I²C
FlexIO01 Out / SCLK I/O
FlexIO02 Out / MOSI I/O
FlexIO03 In / MISO I/O
FlexIO04 In I/O
FlexIO05 Out/♥ / CS* -
EnableFlexOs 1 (default) 0
* Alternate/Additional SPI chip select(s) by means of UserIO(s)
S* of X6 and MH* of X5, as of Rev04½, are left NC to avoid GND links via the FP!
Out-SR: ~20Ω
TODO: Ext. pull-down R?
NB: 3V3 signal
NB: Push/pull!
Protection of 3V3isoIOs for internal and external 3V3 rails
U_FPC-isoIOs-Power_Protection_AP22653
FPC-isoIOs-Power_Protection_AP22653.SchDoc
3V3isoIOs1: I²C-GPIO (0-14 IOs)
3V3isoIOs2: FlexIOs and Outside
External STOP
V_{S-max}: 5.89V (w/o diode drop)
NB for Rev01: LDO ≤100mA
ADUM1250ARZ-RL7
ISO6742FDWR
PCAL9539APW,118
74LVC1T45DW-7
SN6505BDBVR
LDL1117S33R
750316028
M8S-04PFFR-SF8001
DS1037-15FNAKT74-0CC
Title FPC-isoIOs.SchDoc
Revision: 03
Design Engineer: MG & MH
Project: uz_frontpanel_main.PrjPCB
UltraZohm
www.ultrazohm.com
Date: 01/07/2026
Sheet 6 of 36

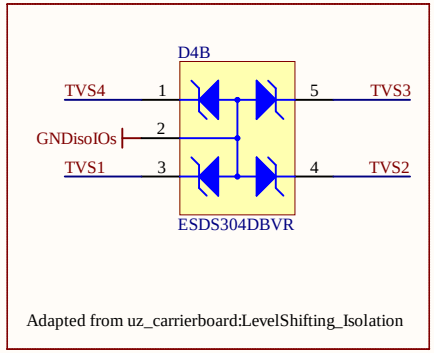




Adapted from uz_carrierboard:LevelShifting_Isolation

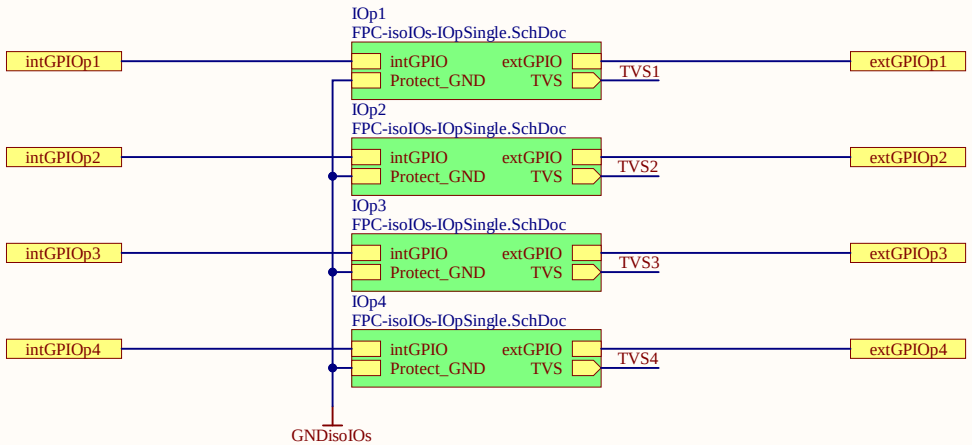
Title FPC-isoIOs-IOpQuad.SchDoc		UltraZohm www.ultrazohm.com
Revision: 03	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026 Sheet 7.1 of 36

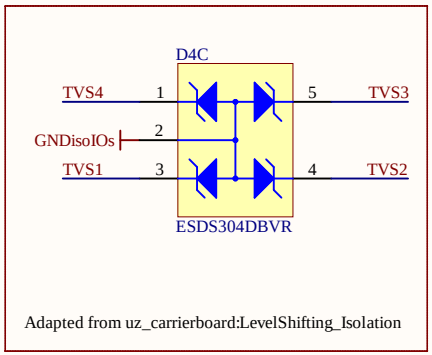




Adapted from uz_carrierboard:LevelShifting_Isolation

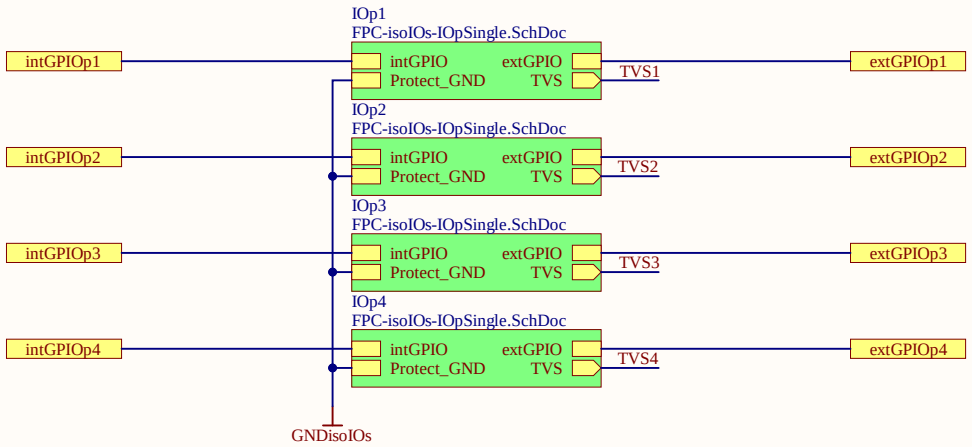
Title FPC-isoIOs-IOpQuad.SchDoc		UltraZohm	
Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 7.2 of 36	

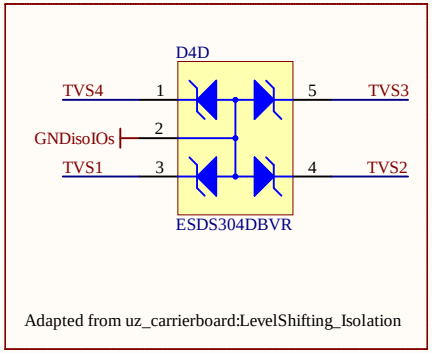




Adapted from uz_carrierboard:LevelShifting_Isolation

Title FPC-isoIOs-IOpQuad.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 03	Design Engineer: MG & MH		
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 7.3 of 36	



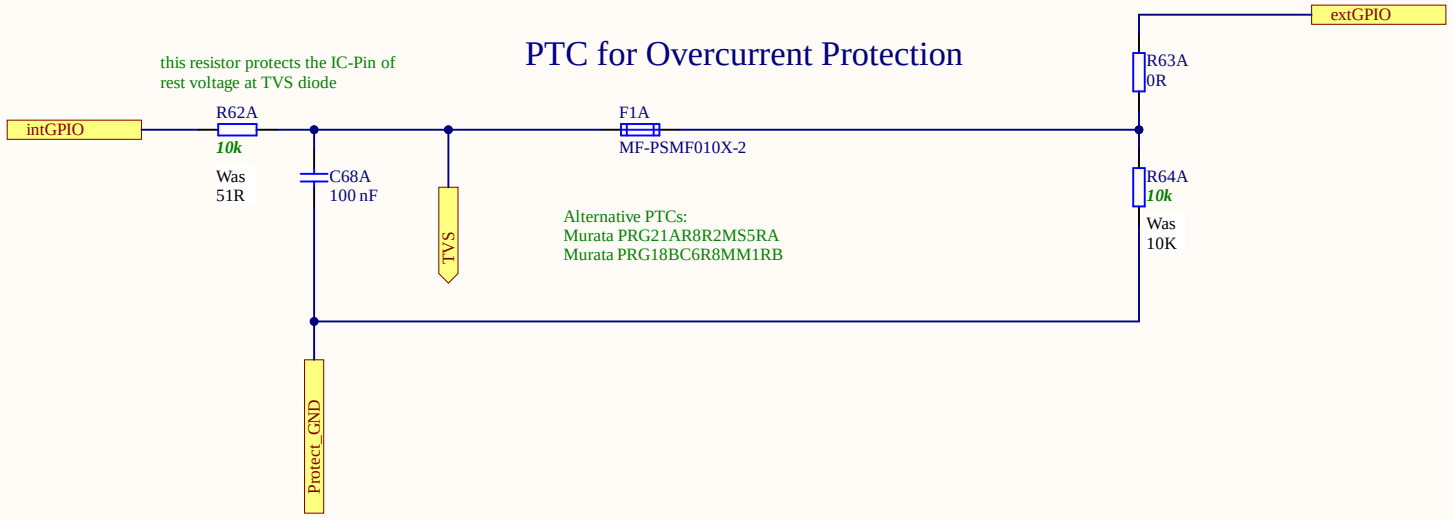


Adapted from uz_carrierboard:LevelShifting_Isolation

Title FPC-isoIOs-IOpQuad.SchDoc		UltraZohm www.ultrazohm.com
Revision: 03	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026 Sheet 7.4 of 36

Voltage Divider

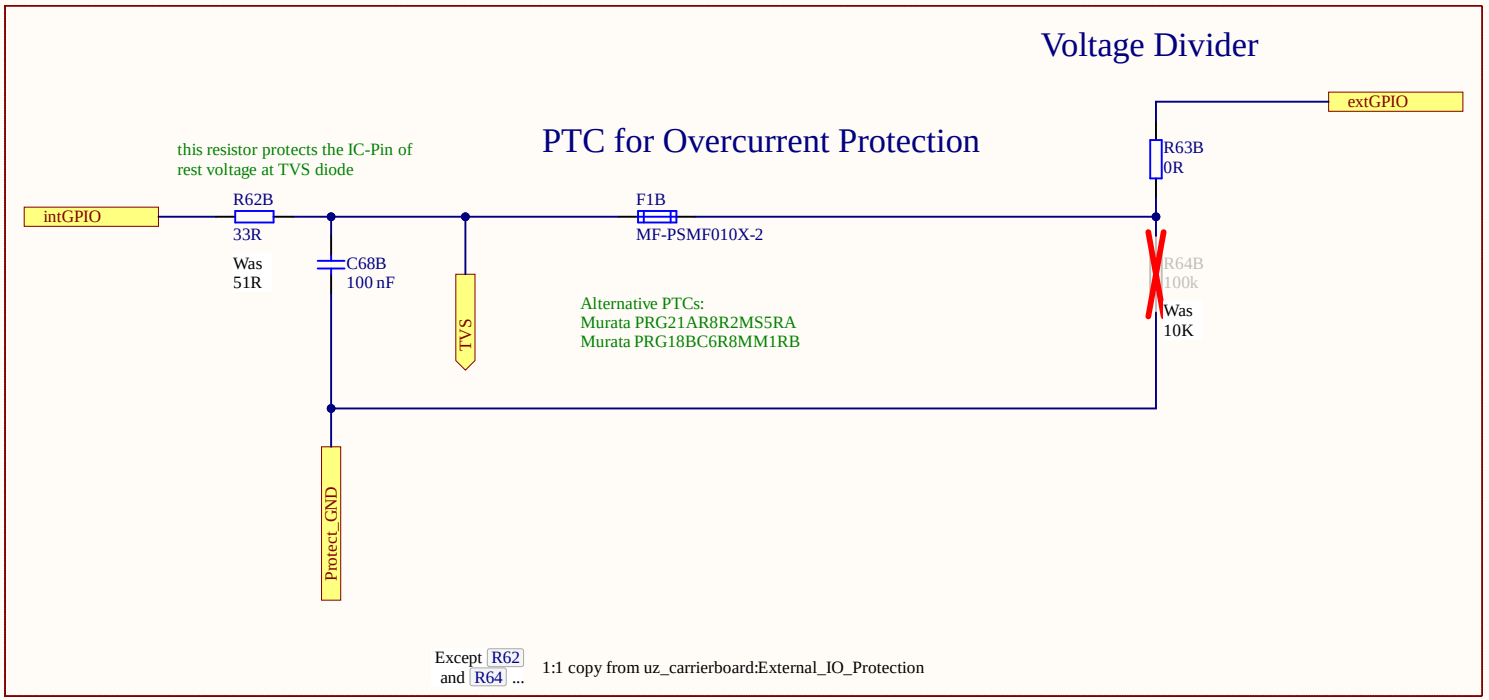
PTC for Overcurrent Protection



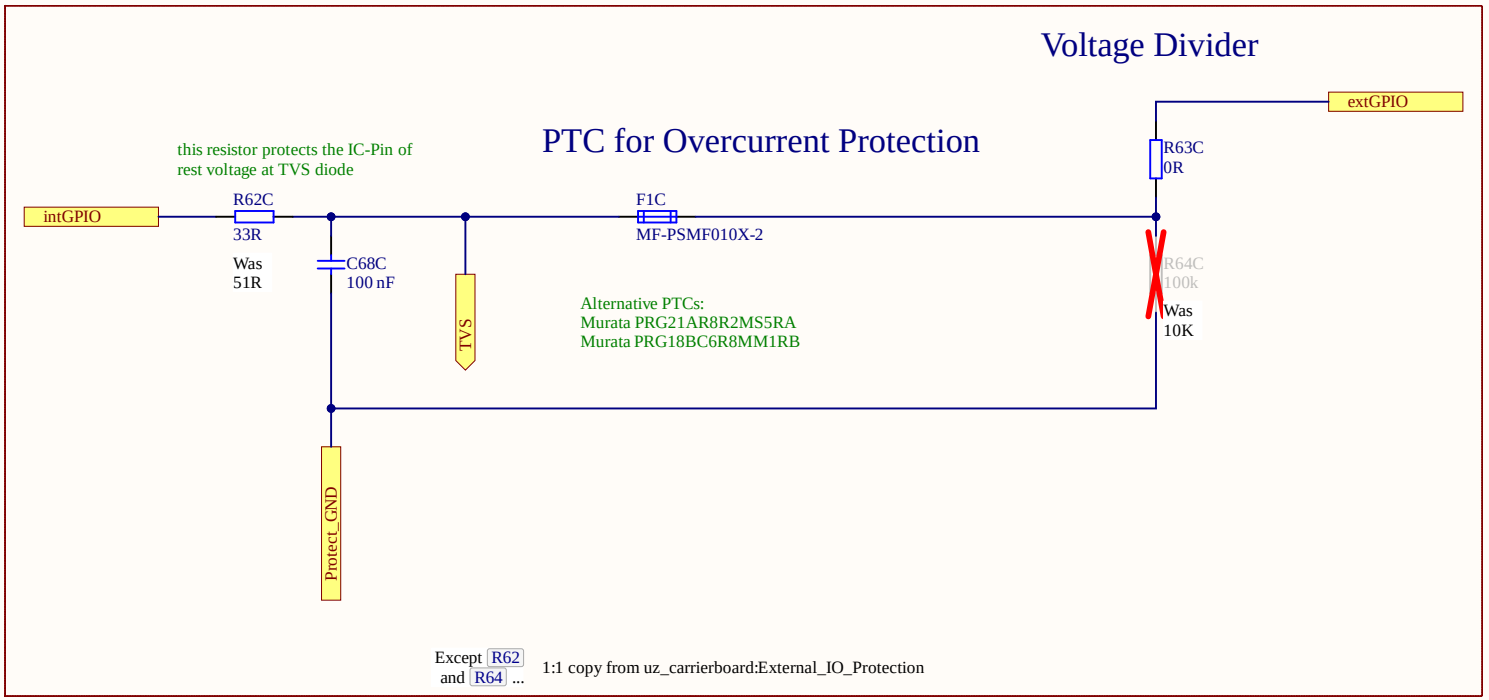
Except R62 and R64 ...

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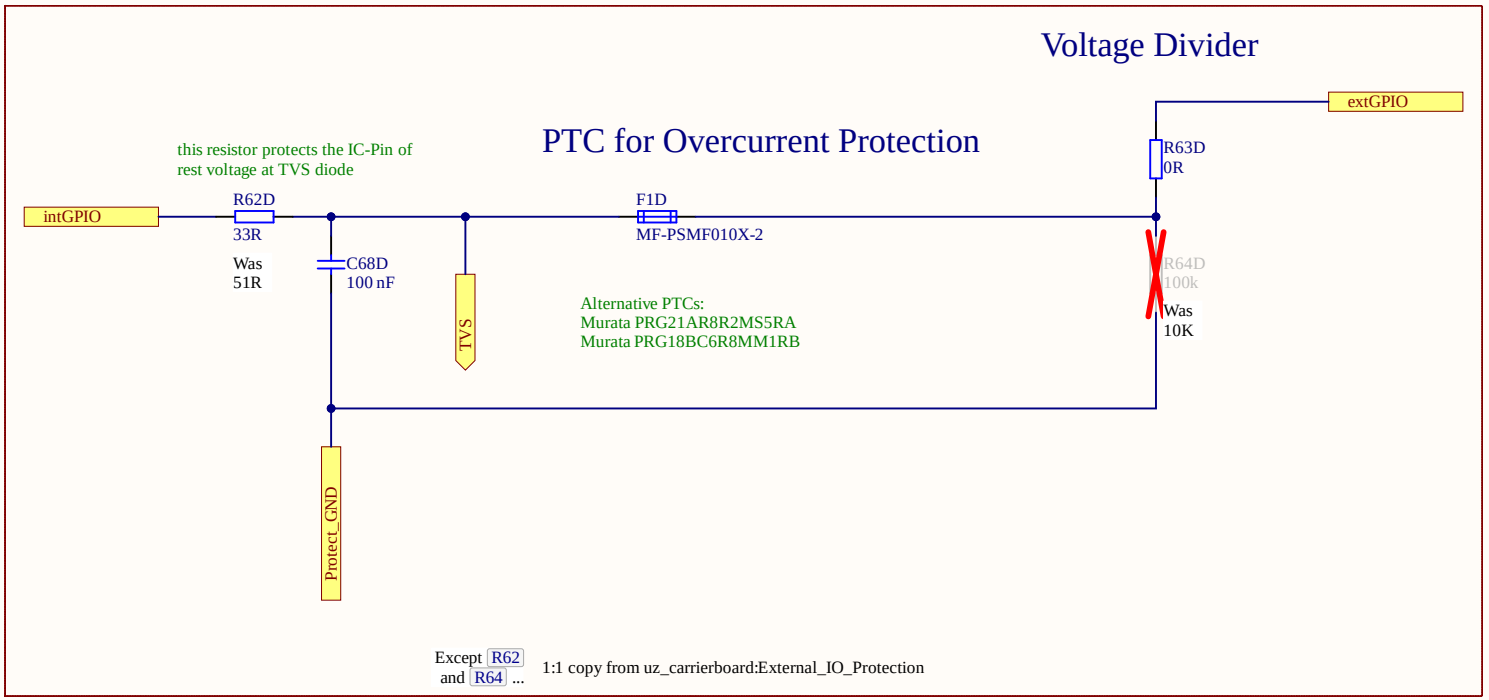
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm www.ultrazohm.com
Revision: 03	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026
		Sheet 8.1.1 of 36



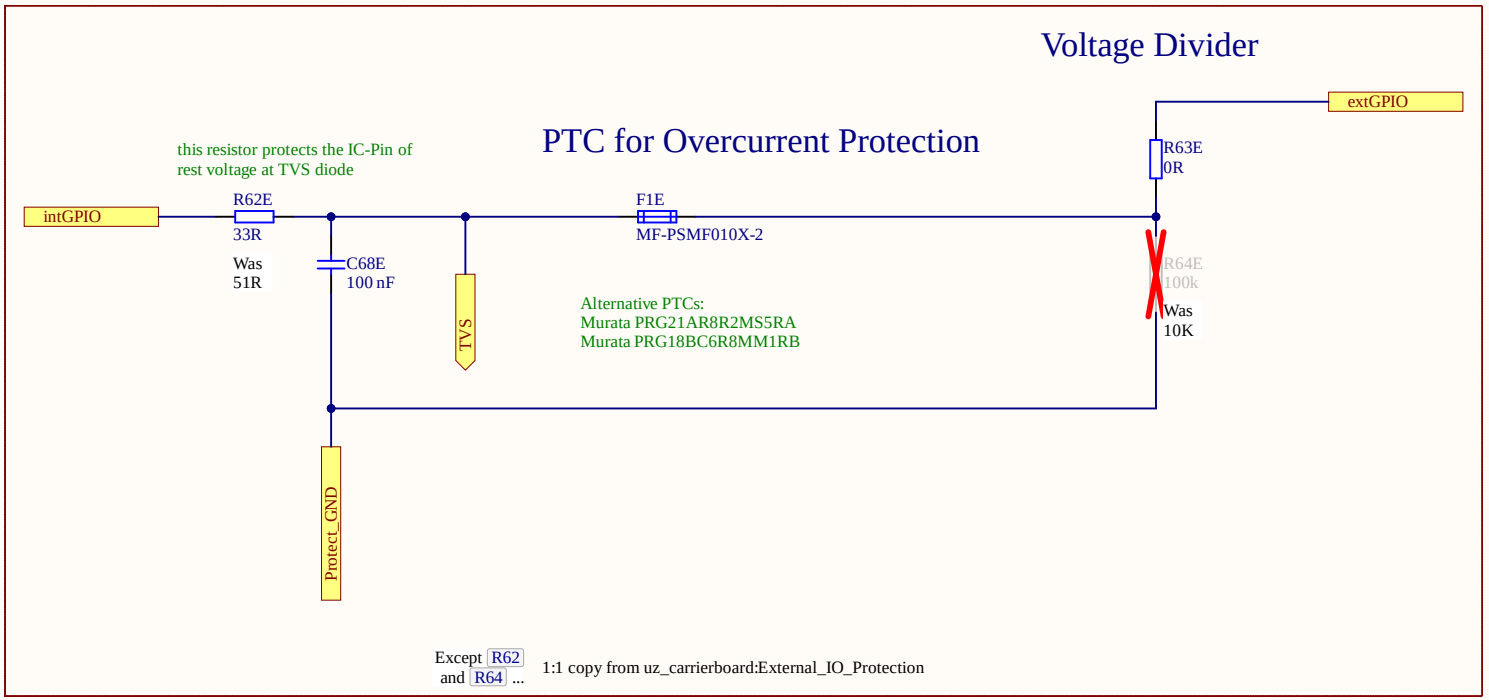
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 8.1.2 of 36	



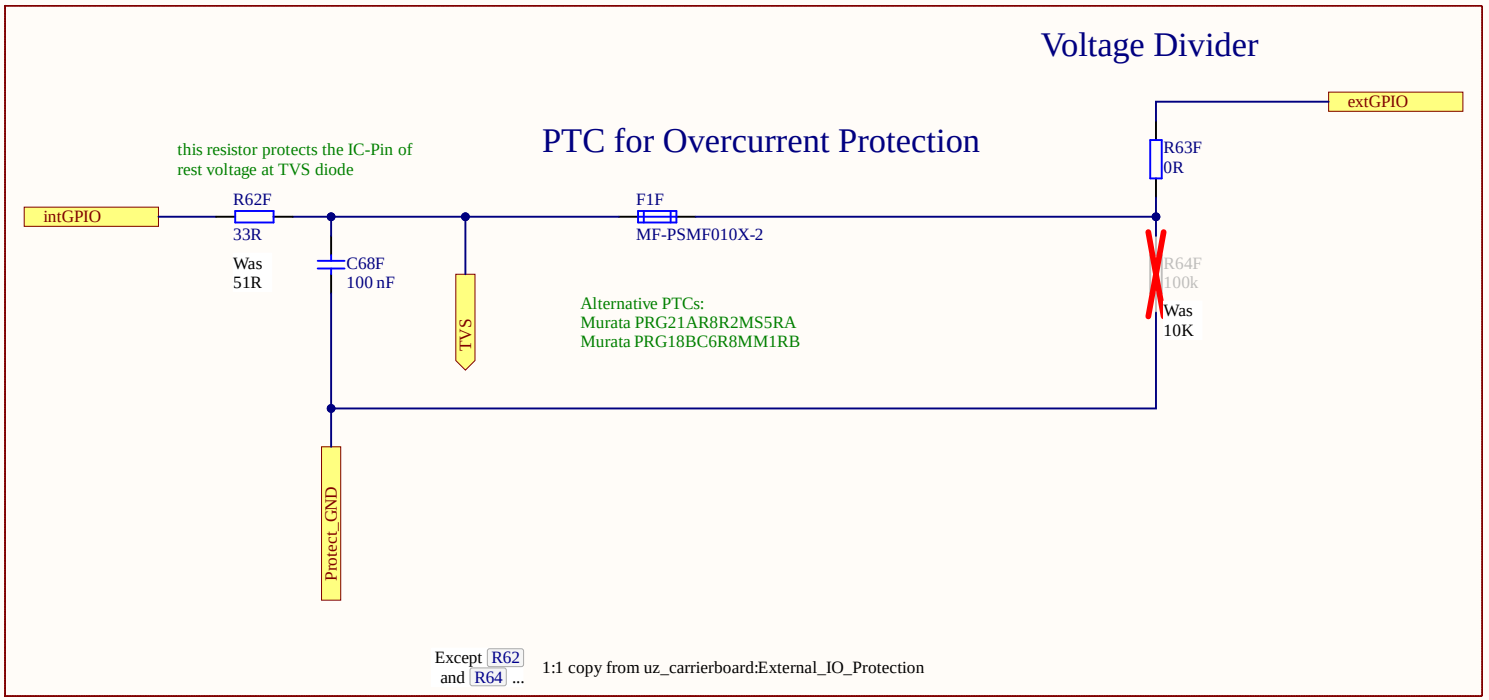
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Revision: 03	Design Engineer: MG & MH		
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 8.1.3 of 36	



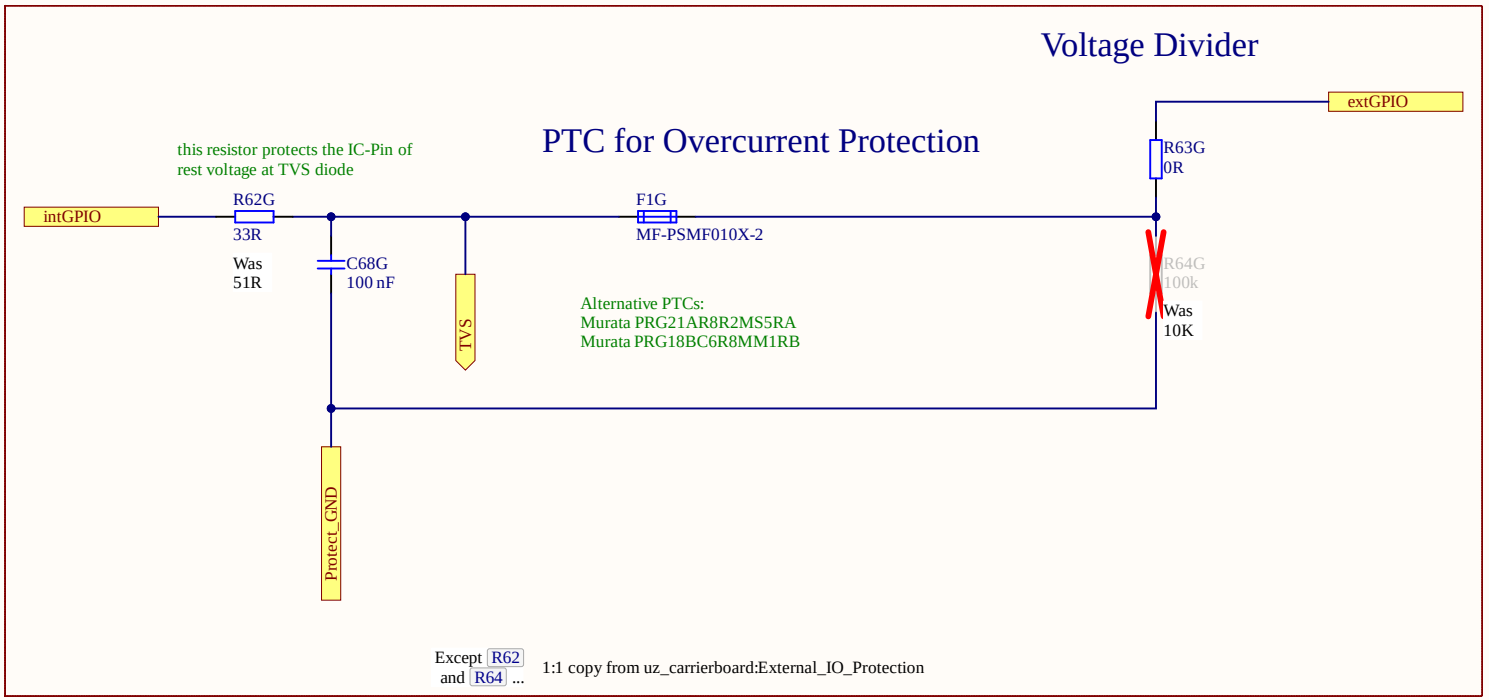
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Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 8.1.4 of 36	



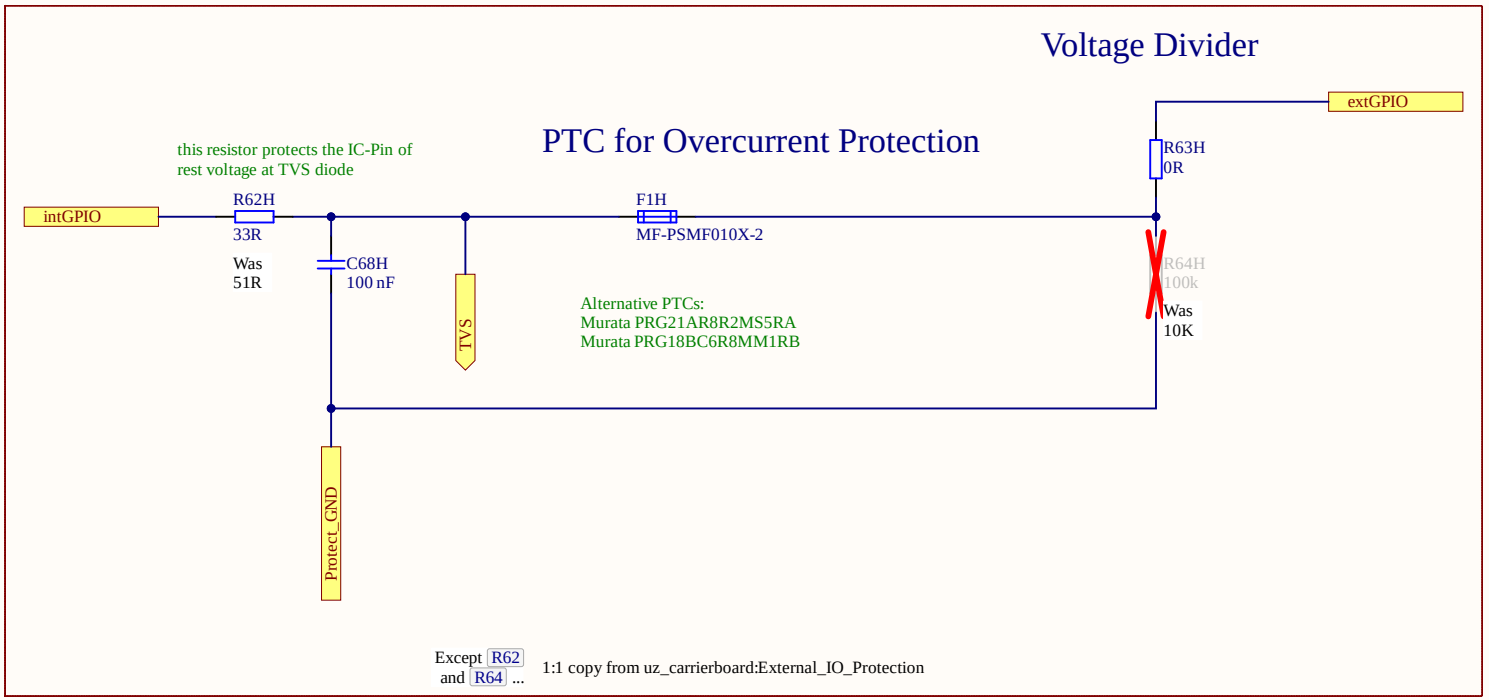
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Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 8.2.1 of 36	



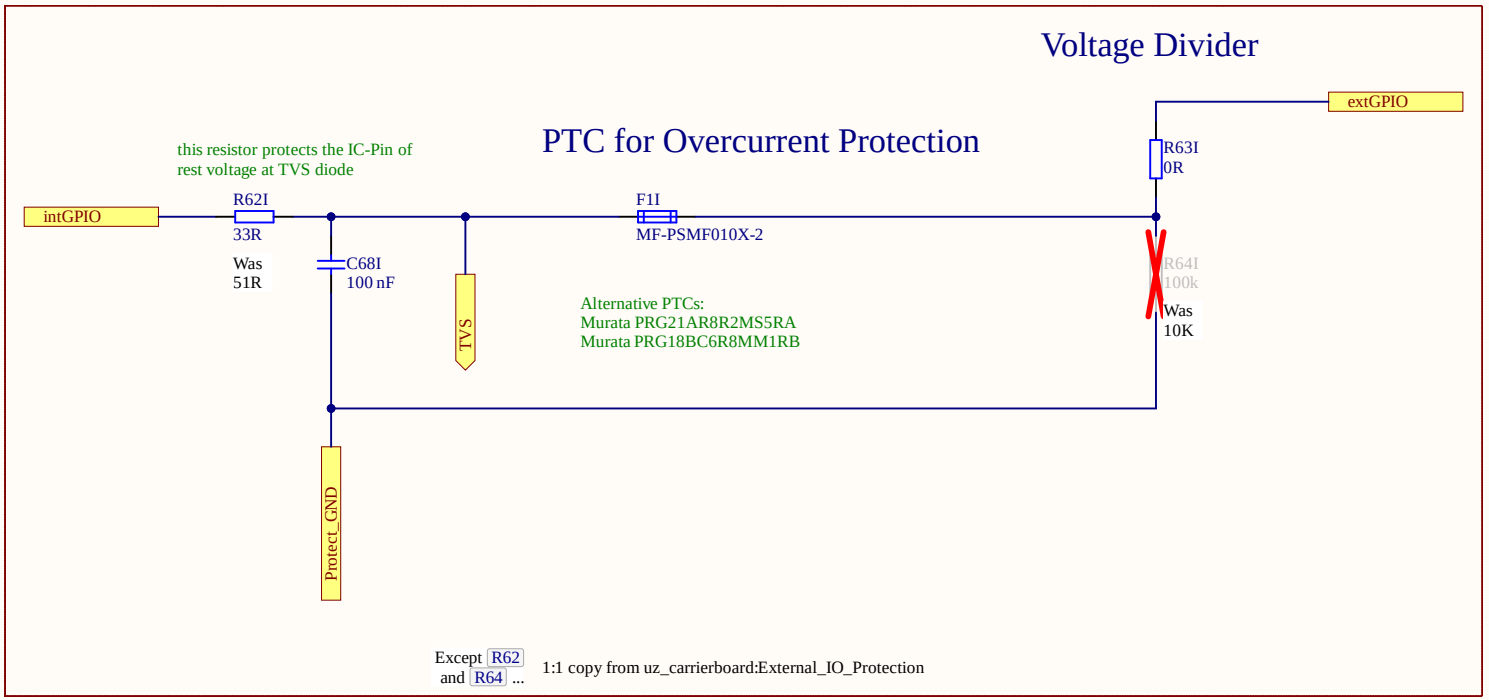
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Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 8.2.2 of 36	



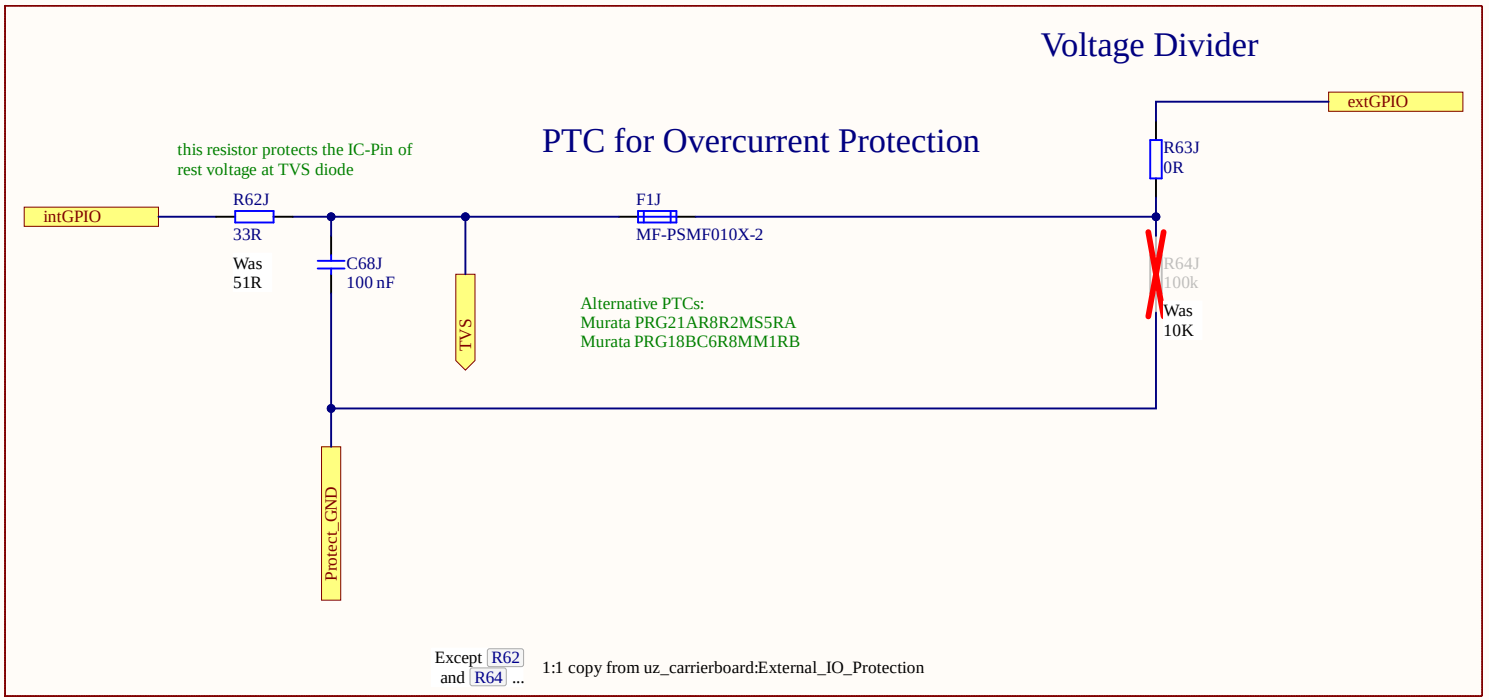
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 03	Design Engineer: MG & MH		
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 8.2.3 of 36	



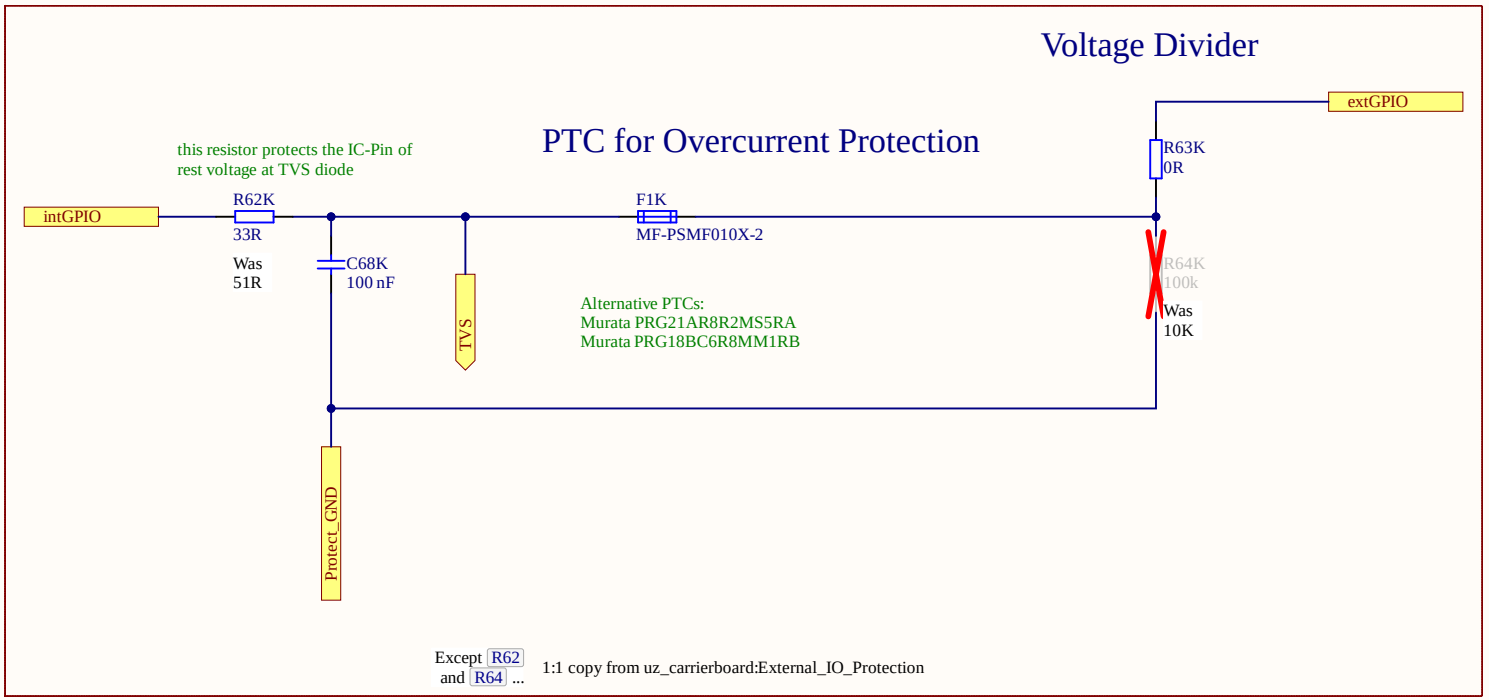
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Revision: 03	Design Engineer: MG & MH		
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 8.2.4 of 36	



Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 8.3.1 of 36	

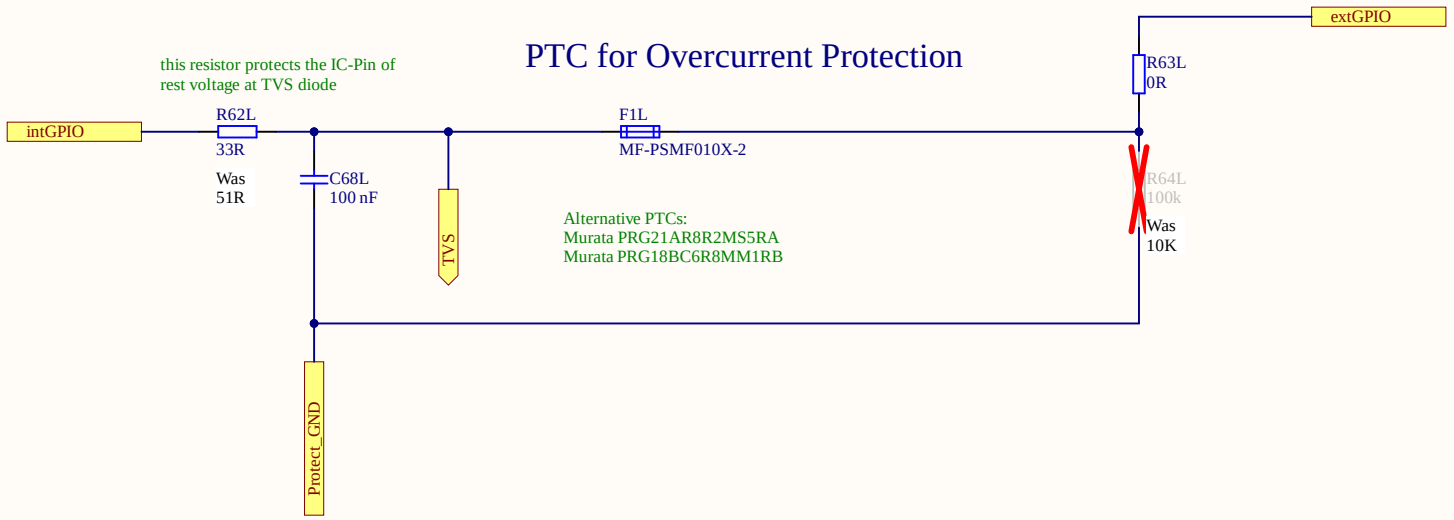


Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 8.3.2 of 36	



Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 03	Design Engineer: MG & MH		
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 8.3.3 of 36	

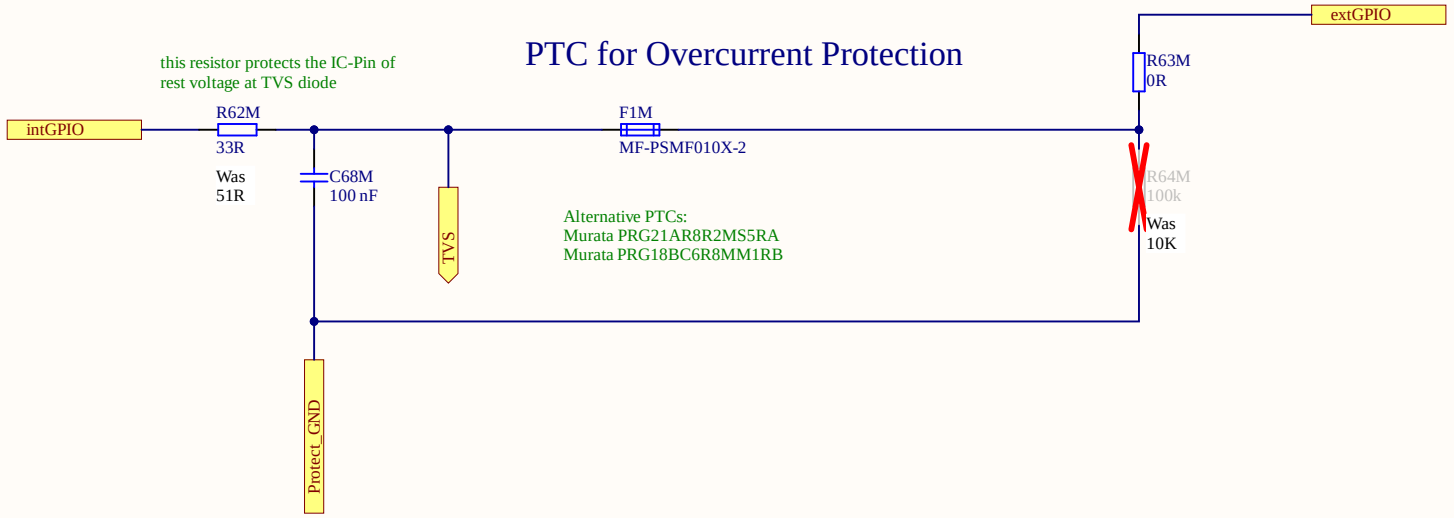
Voltage Divider



Except R62 and R64 ... 1:1 copy from uz_carrierboard:External_IO_Protection

Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm www.ultrazohm.com
Revision: 03	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026 Sheet 8.3.4 of 36

Voltage Divider

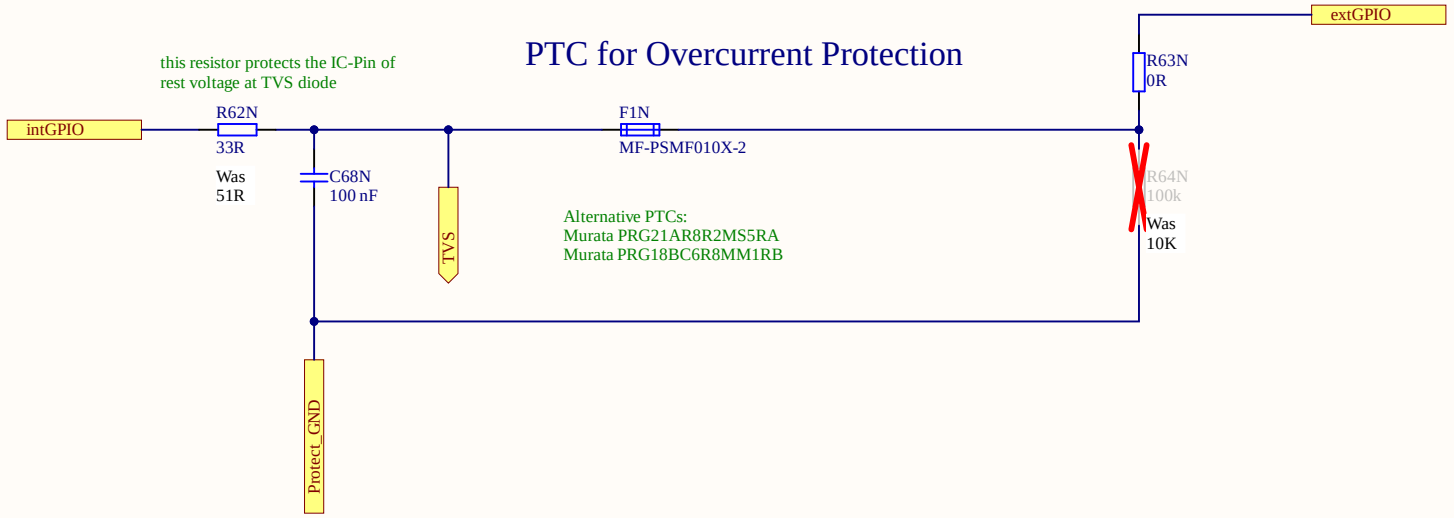


Except R62 and R64 ...

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Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm www.ultrazohm.com
Revision: 03	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026 Sheet 8.4.1 of 36

Voltage Divider

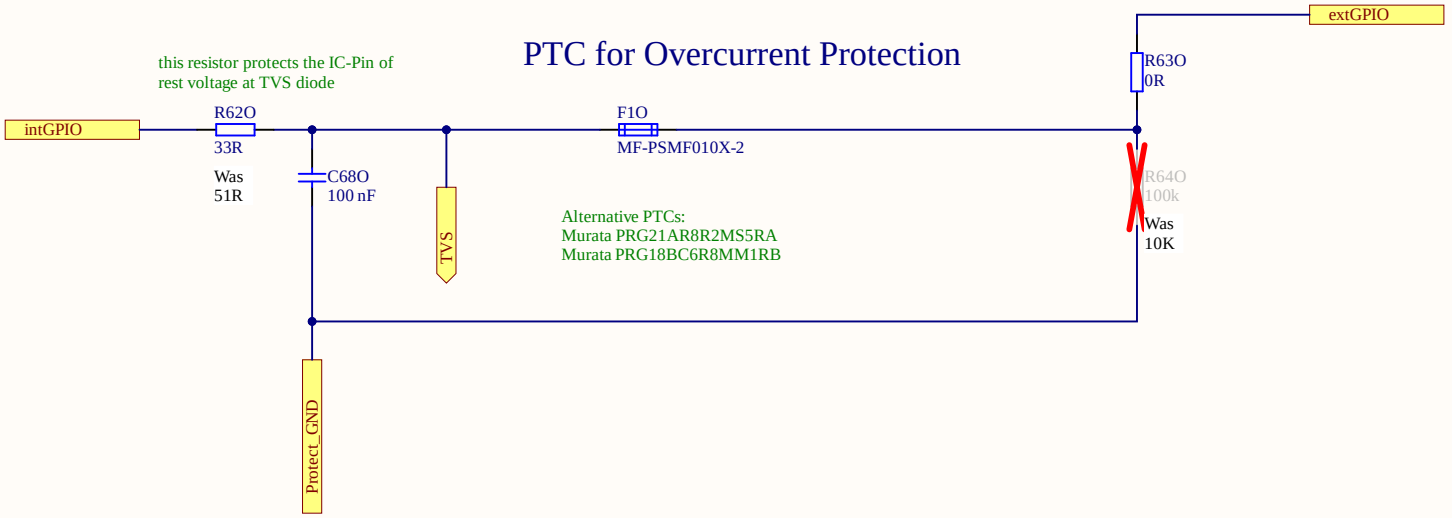


Except R62 and R64 ...

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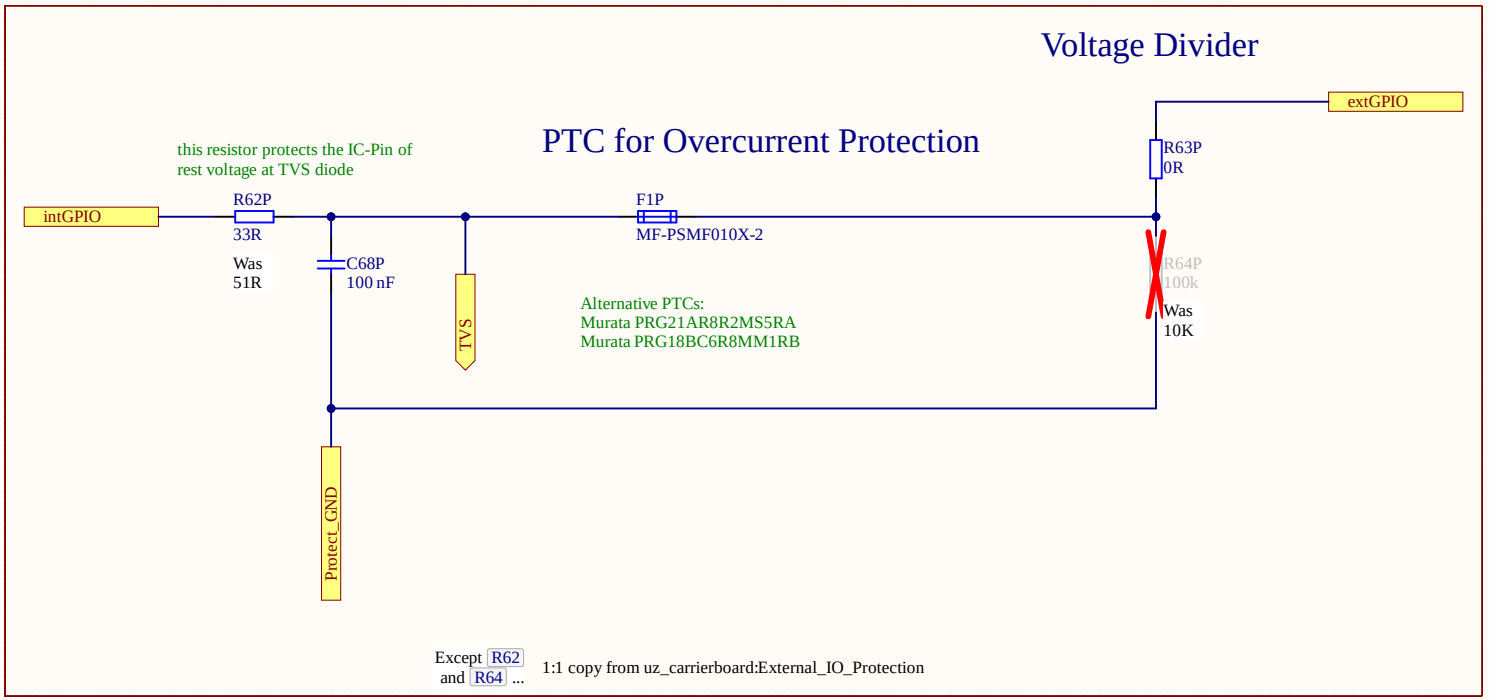
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm www.ultrazohm.com
Revision: 03	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026 Sheet 8.4.2 of 36

Voltage Divider

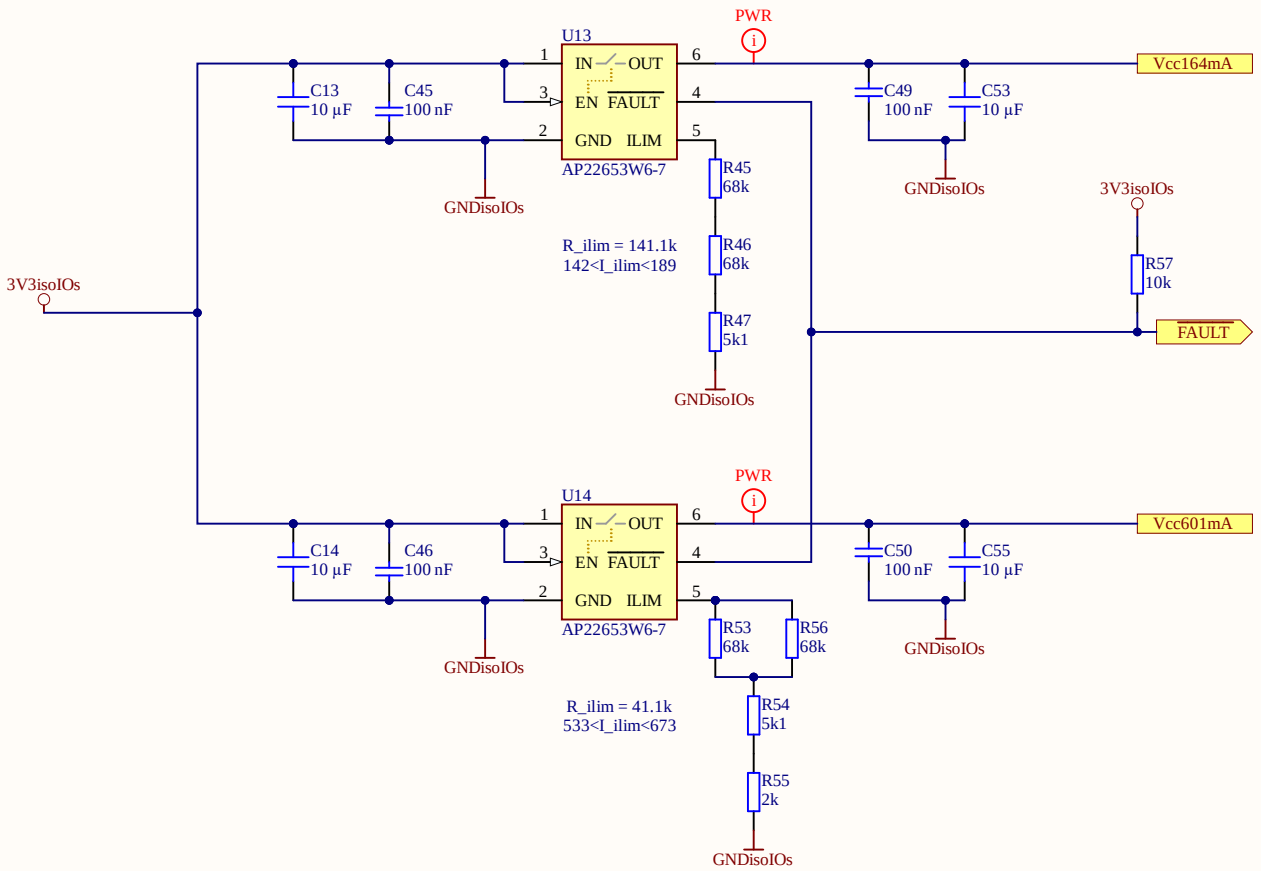


Except R62 and R64 ... 1:1 copy from uz_carrierboard:External_IO_Protection

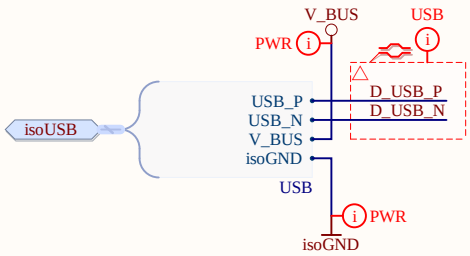
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm www.ultrazohm.com
Revision: 03	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026
		Sheet 8.4.3 of 36



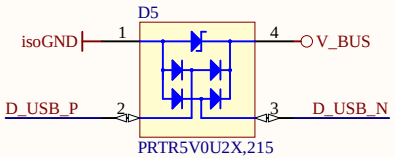
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 8.4.4f 36	

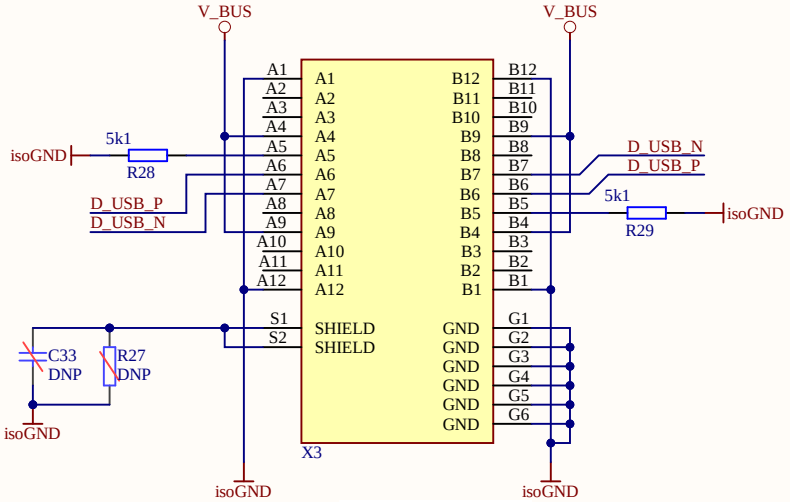


Title FPC-isoIOs-Power_Protection_AP22653.SchDoc		**UltraZohm**	
Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 9 of 36	



Place GND poly on L2





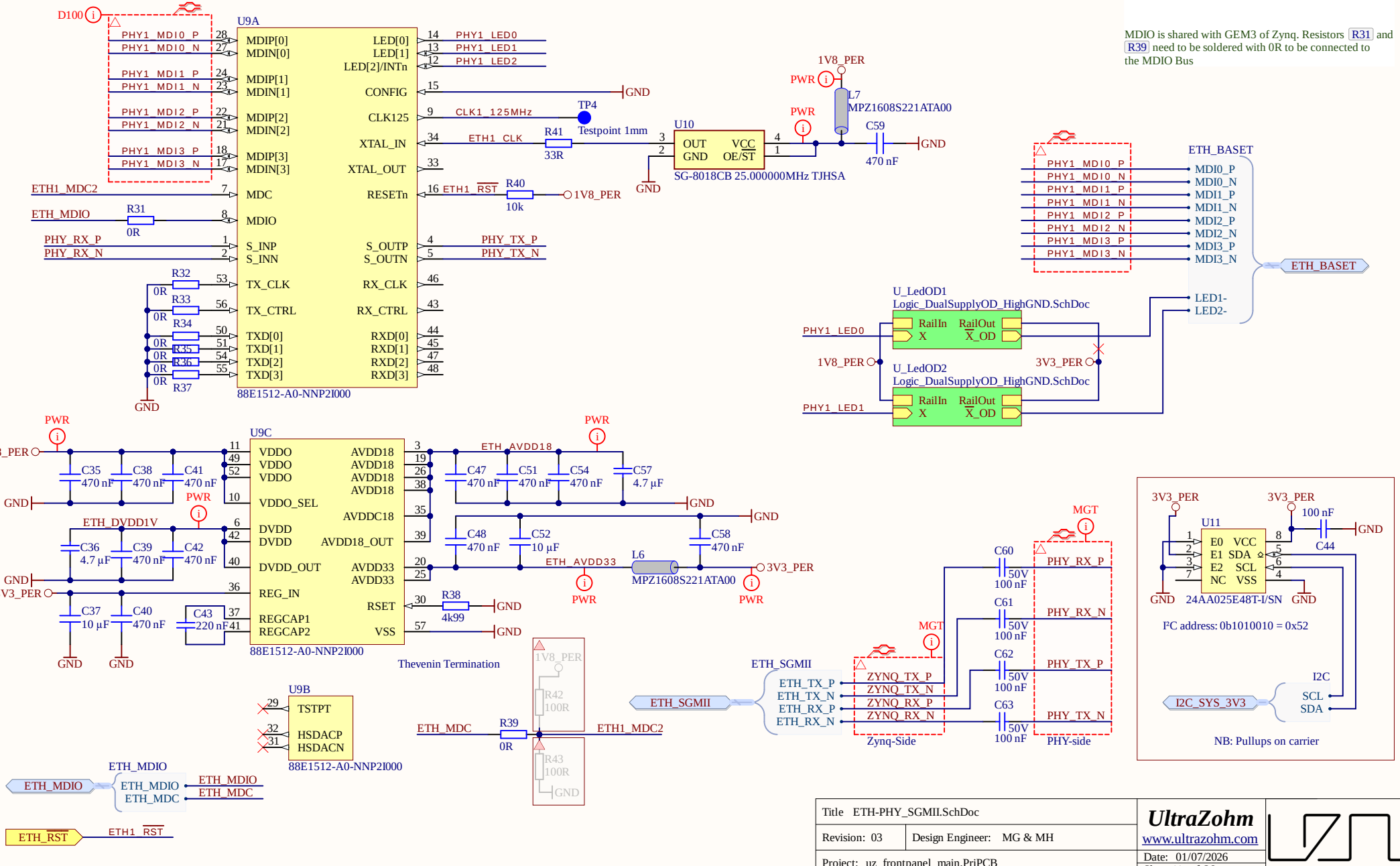
HS USB-C pin assignment:
- A1/B12: GND
- A[23]/B1[10]: SS TX/RX
- A4/B9: VBus
- A5/B5: CC1/2; 5k1 GND
- A6/B6: D+
- A7/B7: D-
- A8/B8: SBU1/2; NC
- A9/B4: VBus
- A1[01]/B[32]: SS TX/RX
- A12/B1: GND

Place GND poly on 3/4 sides

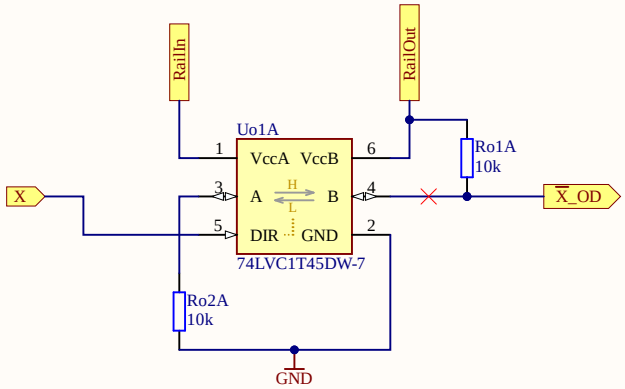
Title FPC-isoJTAG.SchDoc		UltraZohm www.ultrazohm.com
Revision: 03	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026 Sheet 10 of 36

Config Pin 15 is low, so PHY address = 0
PHY is connected to GEM2 of Zynq via SGMII

MDIO is shared with GEM3 of Zynq. Resistors R31 and R39 need to be soldered with 0R to be connected to the MDIO Bus

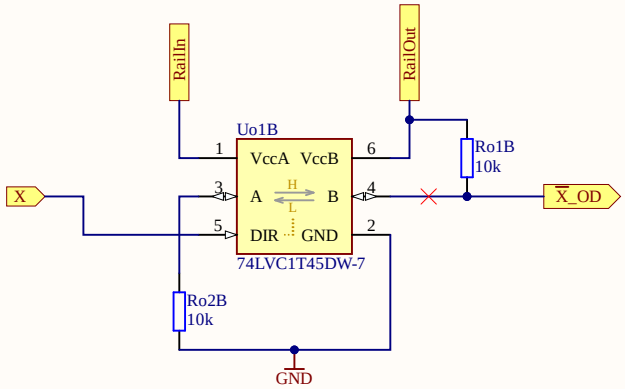


Title ETH-PHY_SGMII.SchDoc		UltraZohm	
Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 11 of 36	



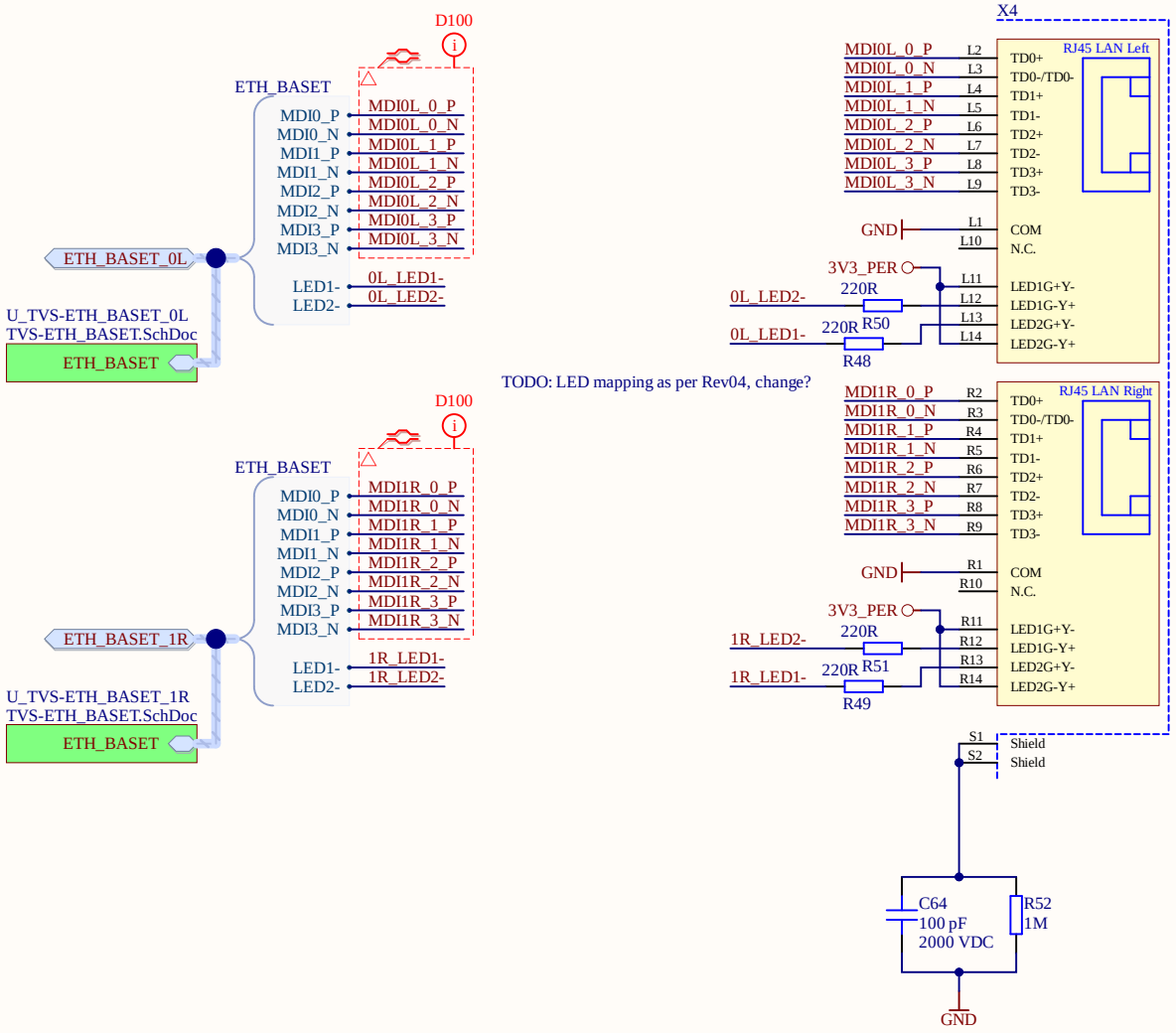
X:	nX_OD:
high	GND
low	Open

Title Logic_DualSupplyOD_HighGND.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 03	Design Engineer: MG & MH		
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 12.1of 36	

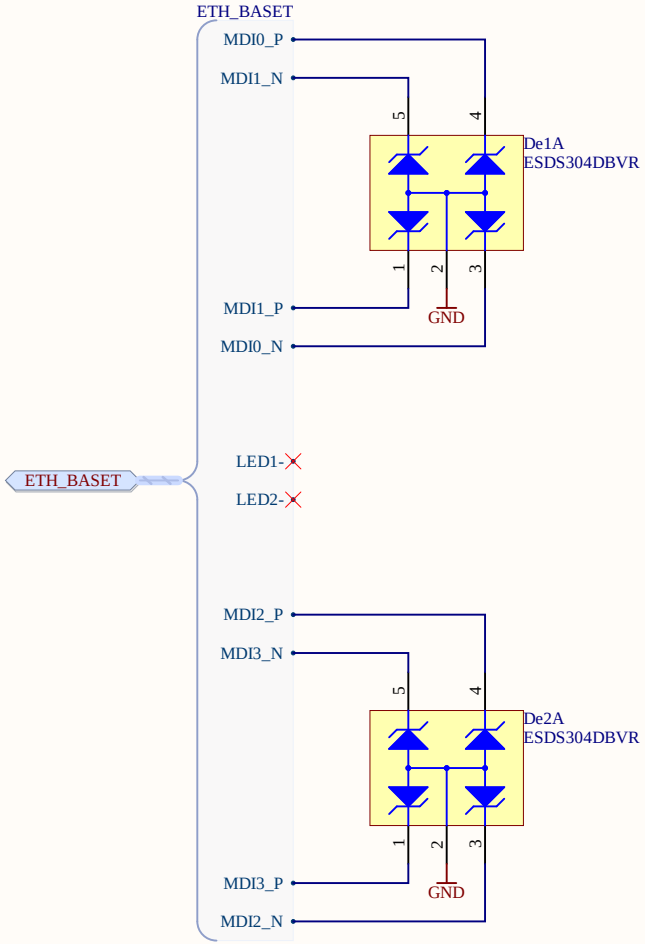


X:	nX_OD:
high	GND
low	Open

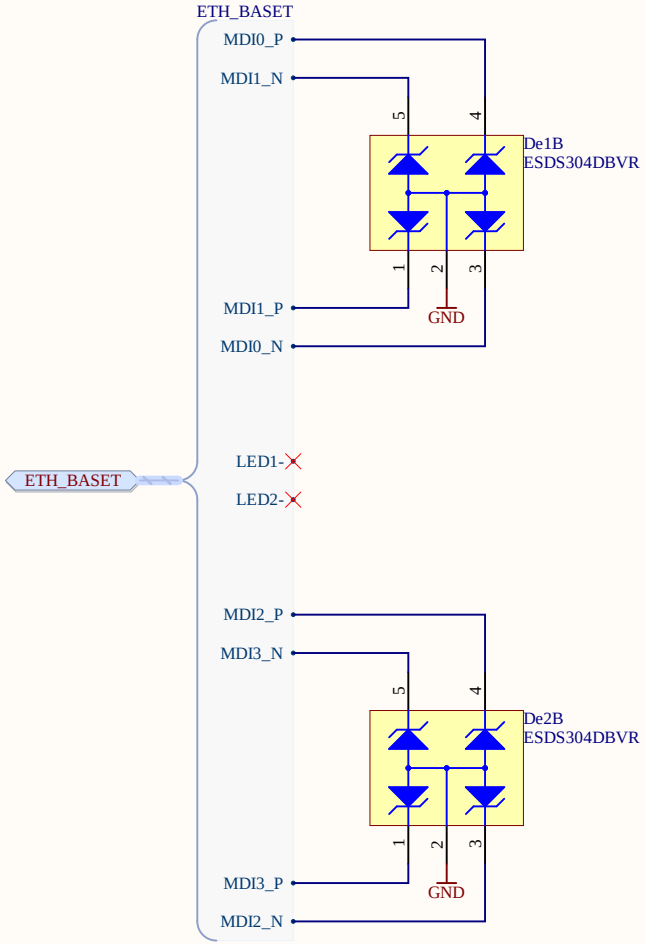
Title	Logic_DualSupplyOD_HighGND.SchDoc	UltraZohm www.ultrazohm.com	
Revision: 03	Design Engineer: MG & MH		
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 12.2 of 36	



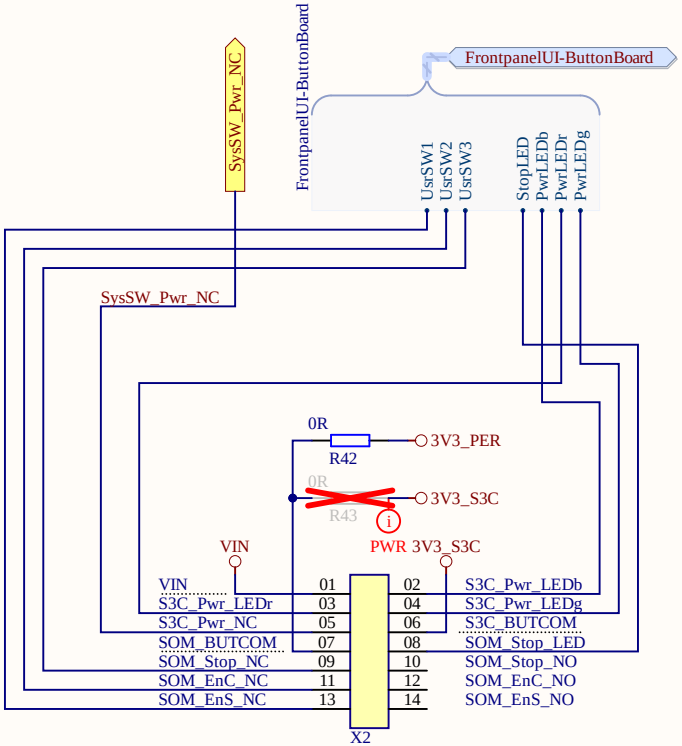
Title FPC-ETH-DualRJ45.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 03	Design Engineer: MG & MH		
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 13 of 36	



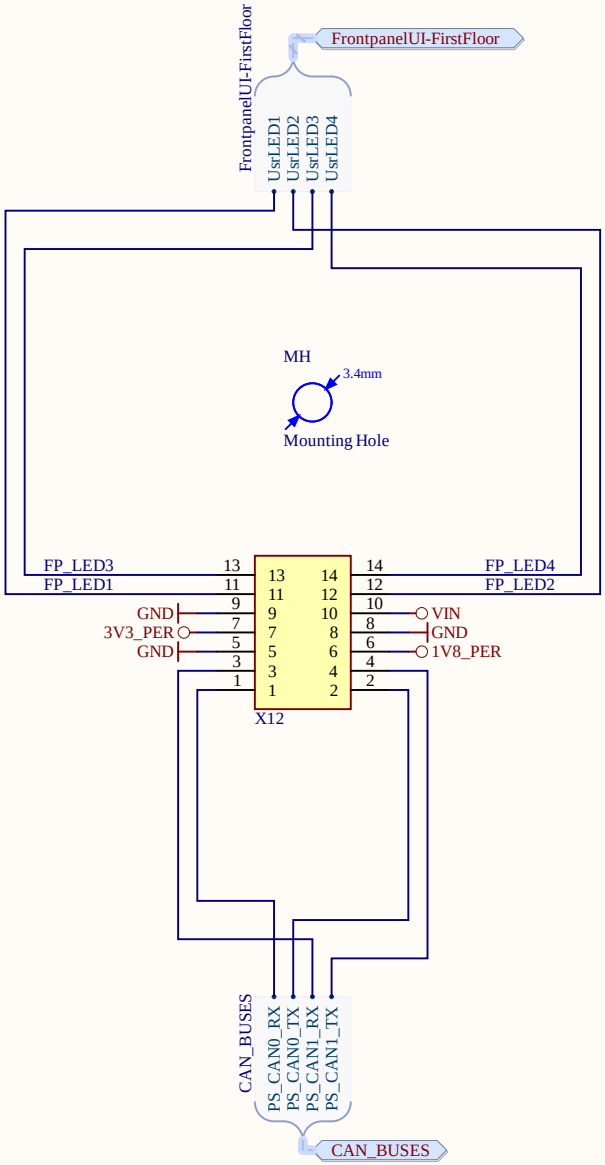
Title TVS-ETH_BASET.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 03	Design Engineer: MG & MH		
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 14.1of 36	



Title TVS-ETH_BASET.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 03	Design Engineer: MG & MH		
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 14.2 of 36	



Title PCB-ButtonBoard.SchDoc		***UltraZohm***	
Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 15 of 36	



Title PCB-FirstFloor.SchDoc		UltraZohm	
Revision: 03	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 01/07/2026	
		Sheet 16 of 36	