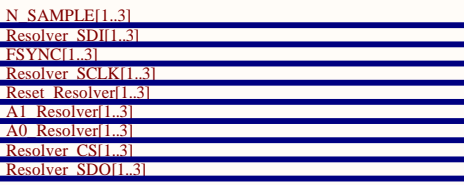
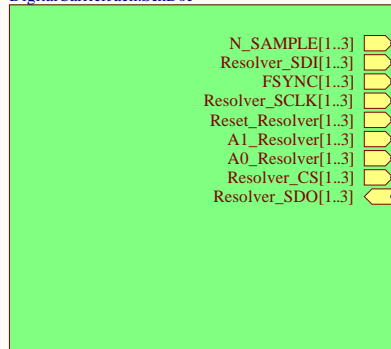
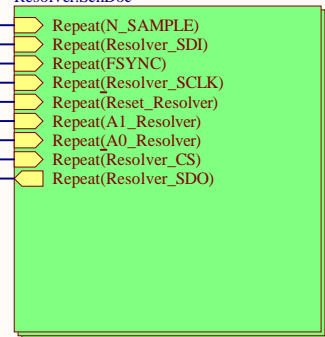


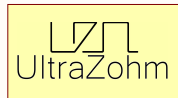
DigitalCarrierJack
DigitalCarrierJack.SchDoc



Repeat(U_Resolver,1,3)
Resolver.SchDoc



Chose size of UZ logo
by chosing footprint
type



LOGO1



LOGO2

UZ_D_Resolver
Project

Martin Bauer
Designer

02/2023
Date

Rev02
Revision

Serial
Serial

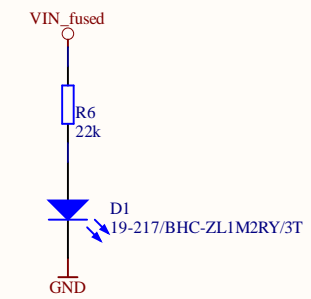
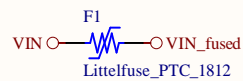
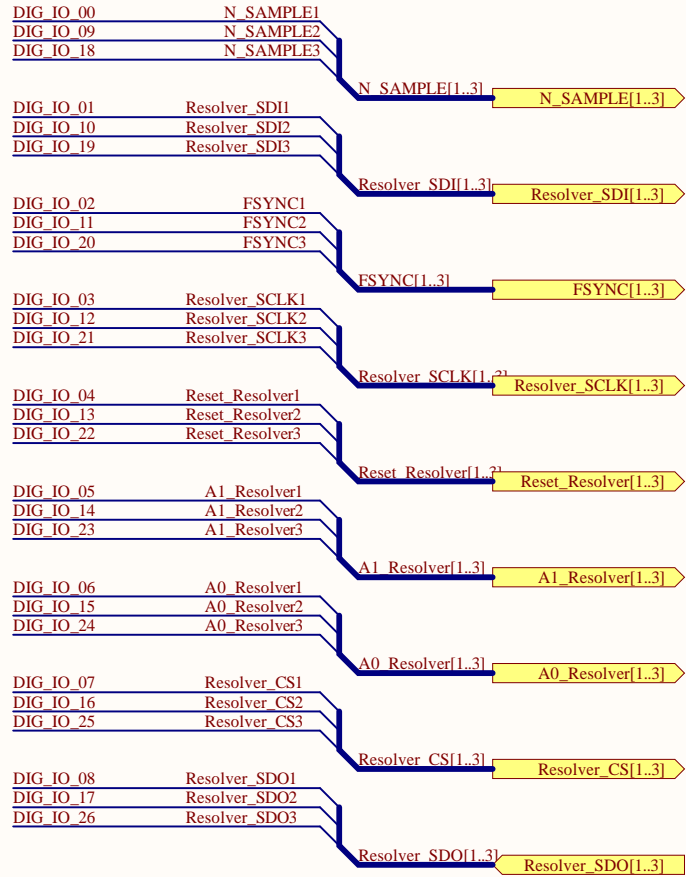
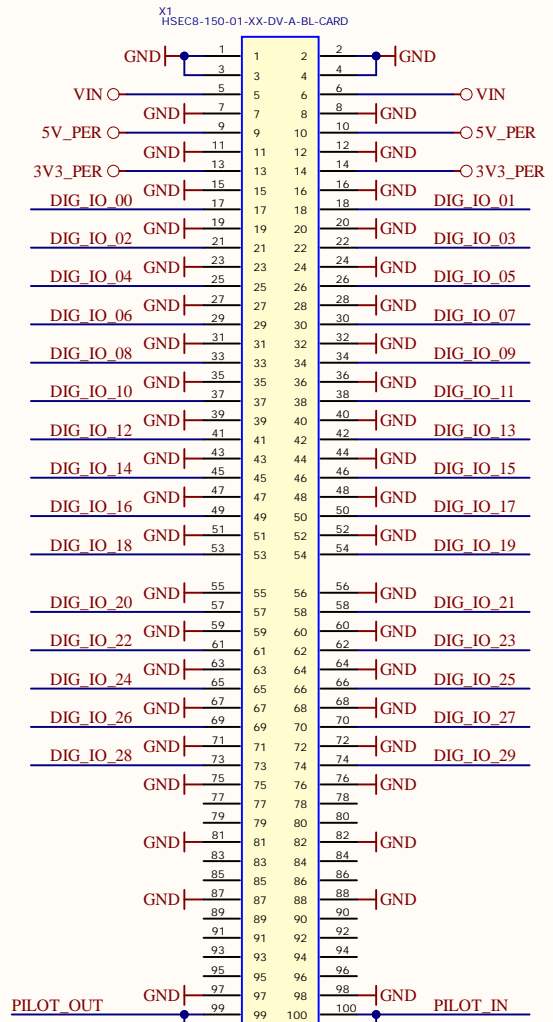
Title TopSheet.SchDoc	
Revision: Rev02	Design Engineer: Martin Bauer
Project: UZ_D_Resolver.PjPCB	

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Date: 20.02.2023
Sheet 1 of 14



A

A

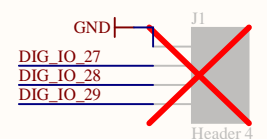


B

B

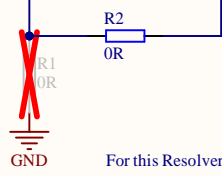
C

C



D

D

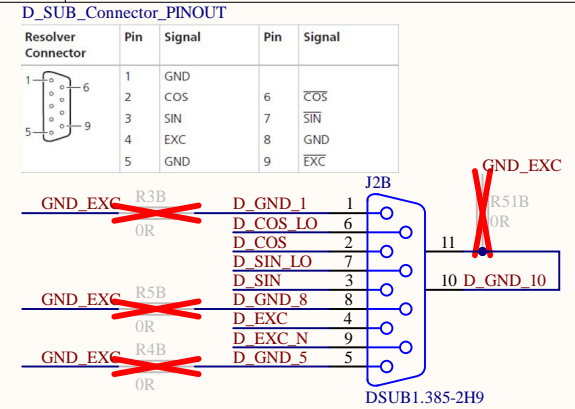
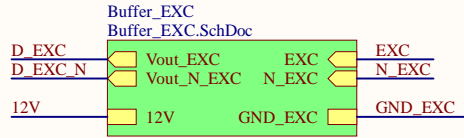
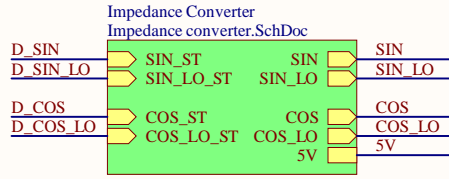
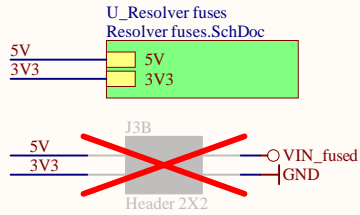


For this Resolver PCB no Collective_FLT (typically 96) is used

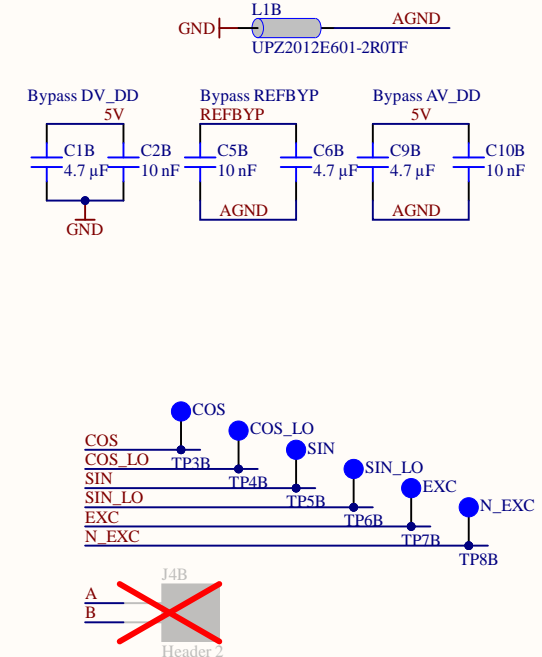
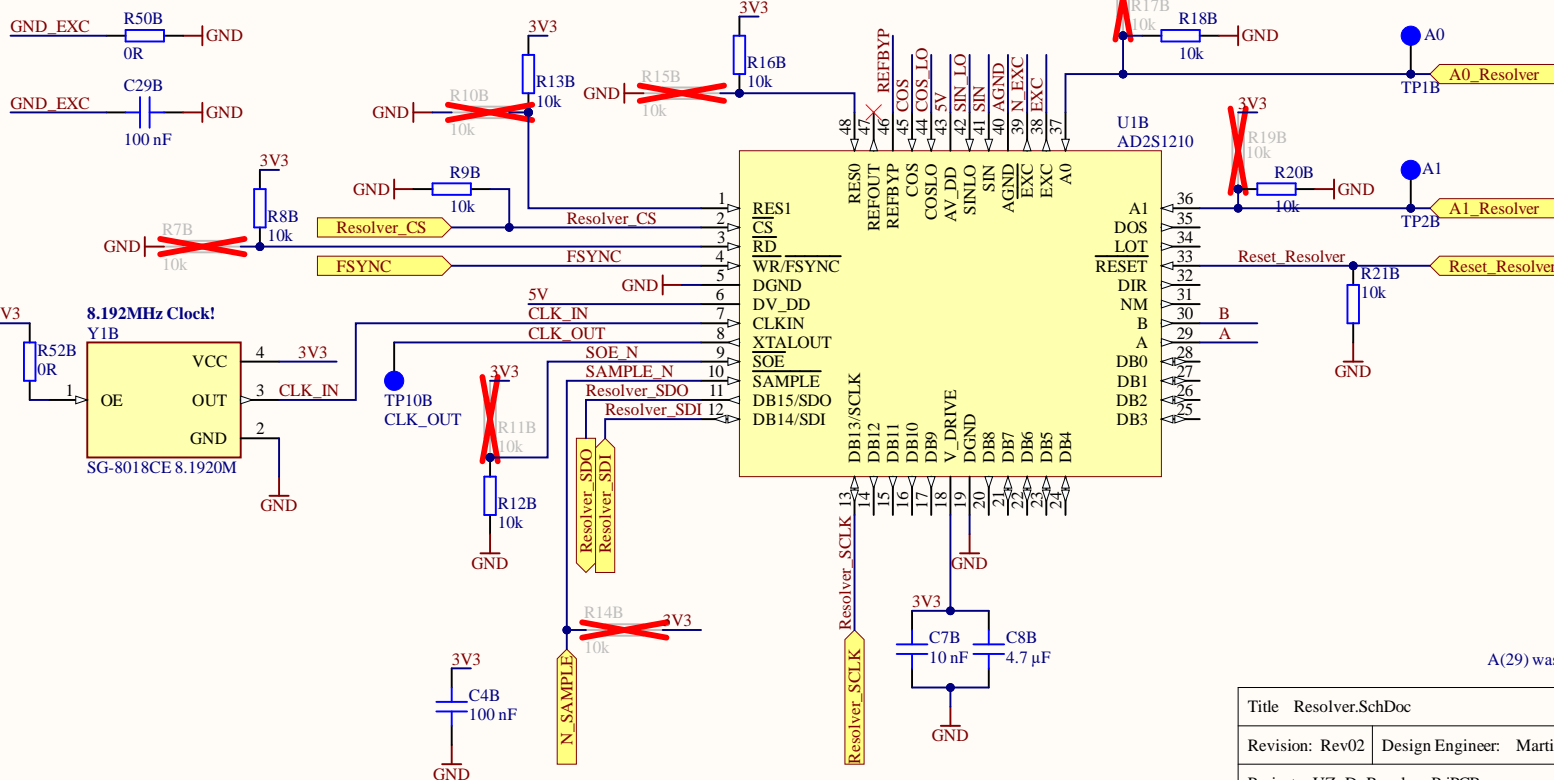
Title DigitalCarrierJack.SchDoc		UltraZohm www.ultrazohm.com	
Revision: Rev02	Design Engineer: Martin Bauer		
Project: UZ_D_Resolver.PjPCB		Date: 20.02.2023	
		Sheet 2 of 14	

RD = HIGH means output buffer disabled, if SOE = LOW -> RD=HIGH
 SOE = LOW means Serial Interface is selected
 RES1 = RES0 = HIGH means 16 bits resolution

Only serial Interface to be used



OPTION separated Ground for Buffer Excitation Circuits / stitching Capacitor

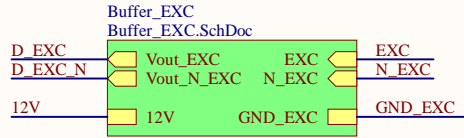
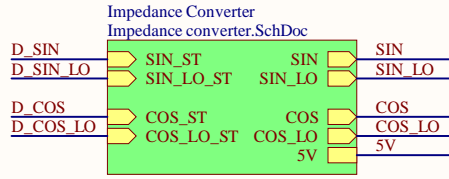
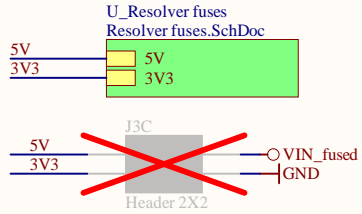


A(29) was redefined as an Output to fix floating PIN Error, as it is unused

Title Resolver.SchDoc		
Revision: Rev02	Design Engineer: Martin Bauer	
Project: UZ_D_Resolver.PjPCB		www.ultrazohm.com Date: 20.02.2023 Sheet 3.2 of 14

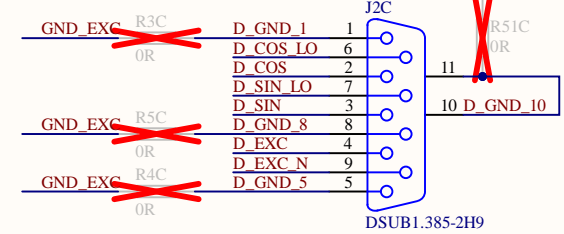
RD = HIGH means output buffer disabled, if SOE = LOW -> RD = HIGH
 SOE = LOW means Serial Interface is selected
 RES1 = RES0 = HIGH means 16 bits resolution

Only serial Interface to be used

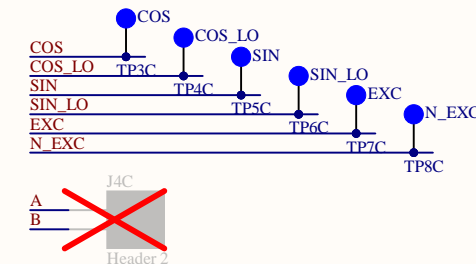
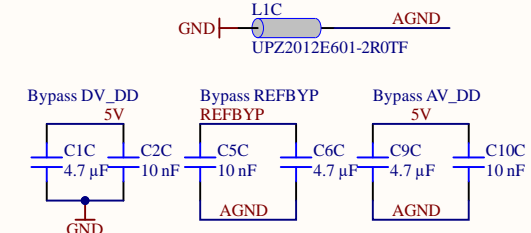
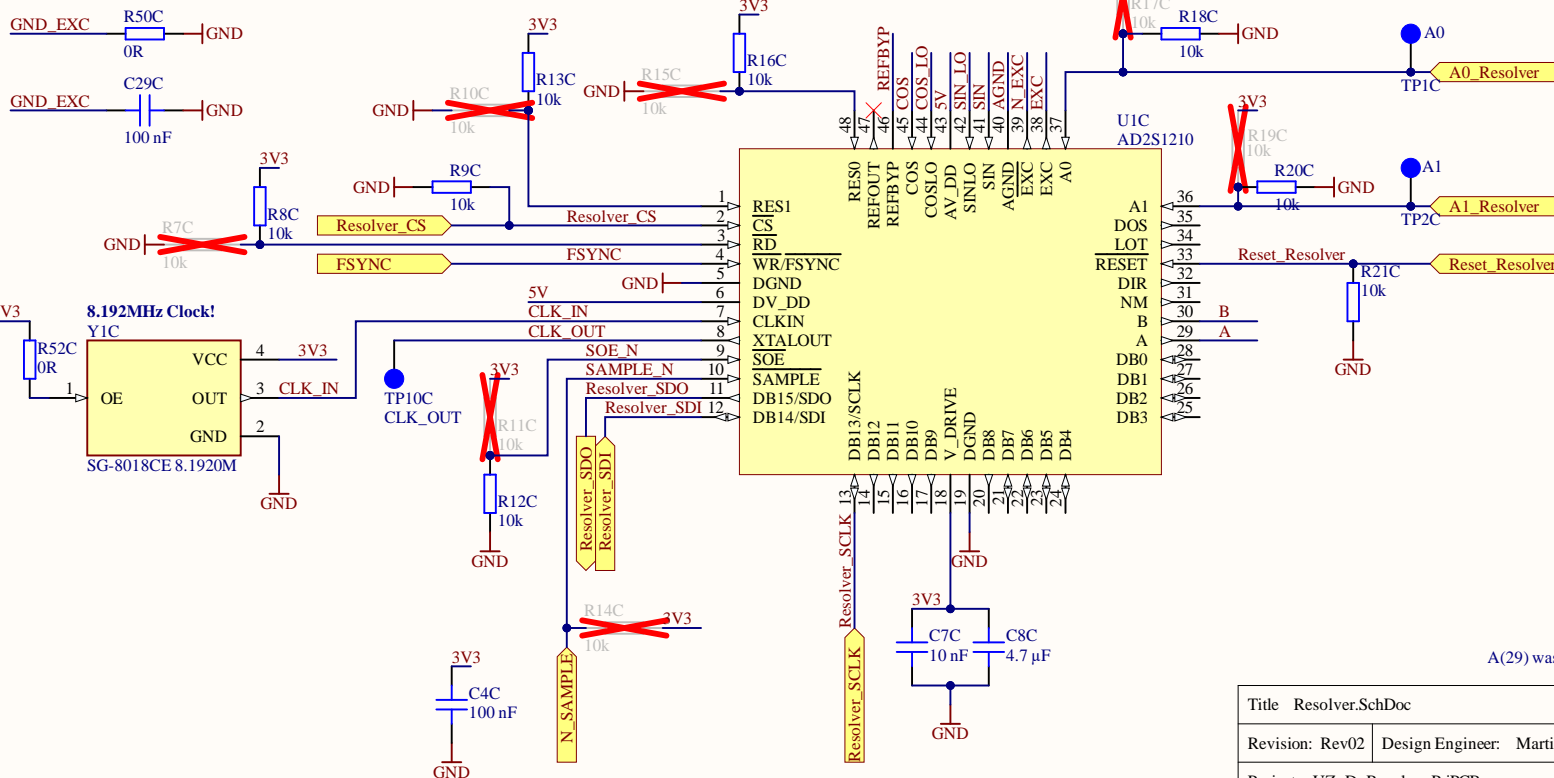


D_SUB_Connector_PINOUT

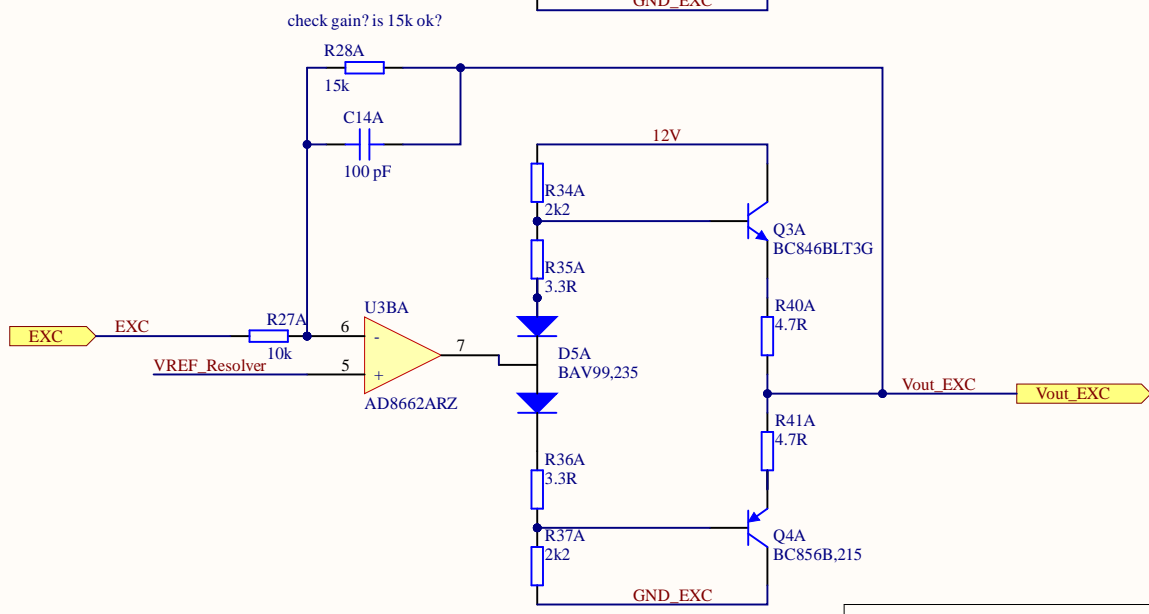
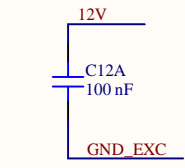
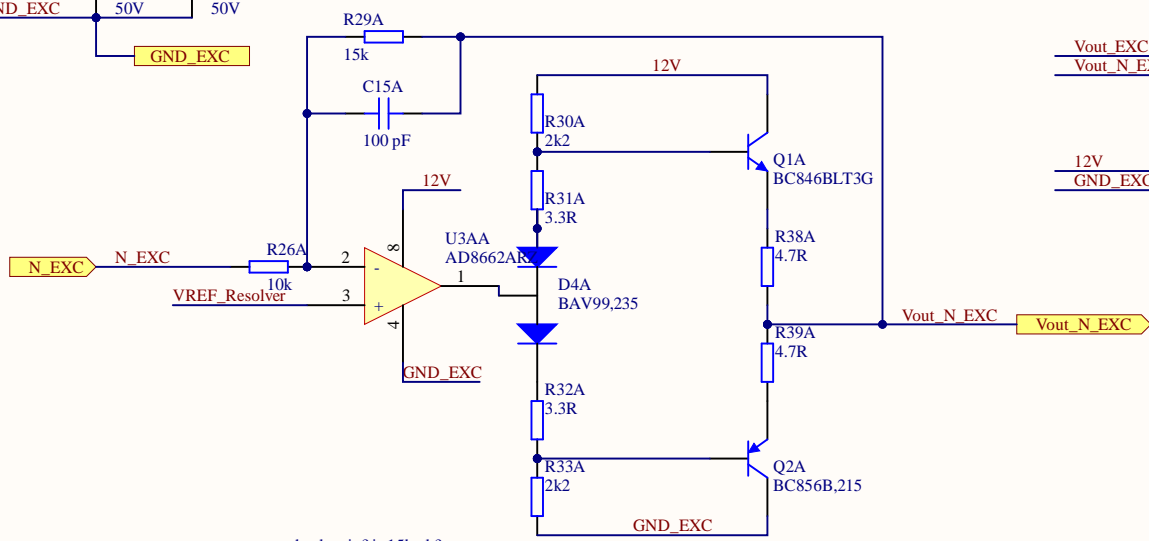
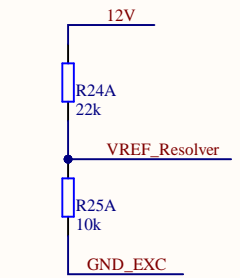
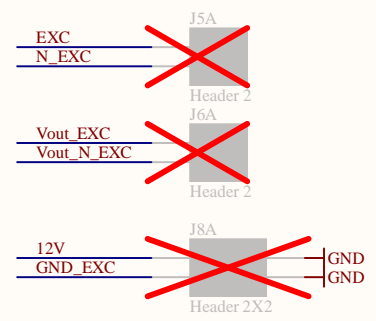
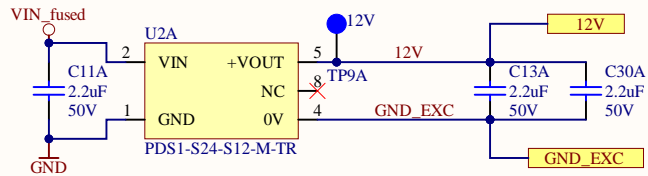
Resolver Connector	Pin	Signal	Pin	Signal
	1	GND	6	COS
	2	COS	7	SIN
	3	SIN	8	GND
	4	EXC	9	EXC
	5	GND		



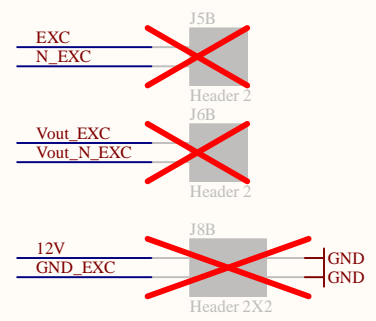
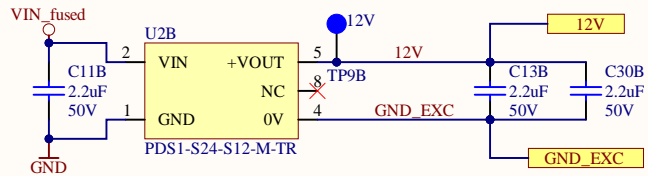
OPTION separated Ground for Buffer Excitation Circuits / stitching Capacitor



A(29) was redefined as an Output to fix floating PIN Error, as it is unused

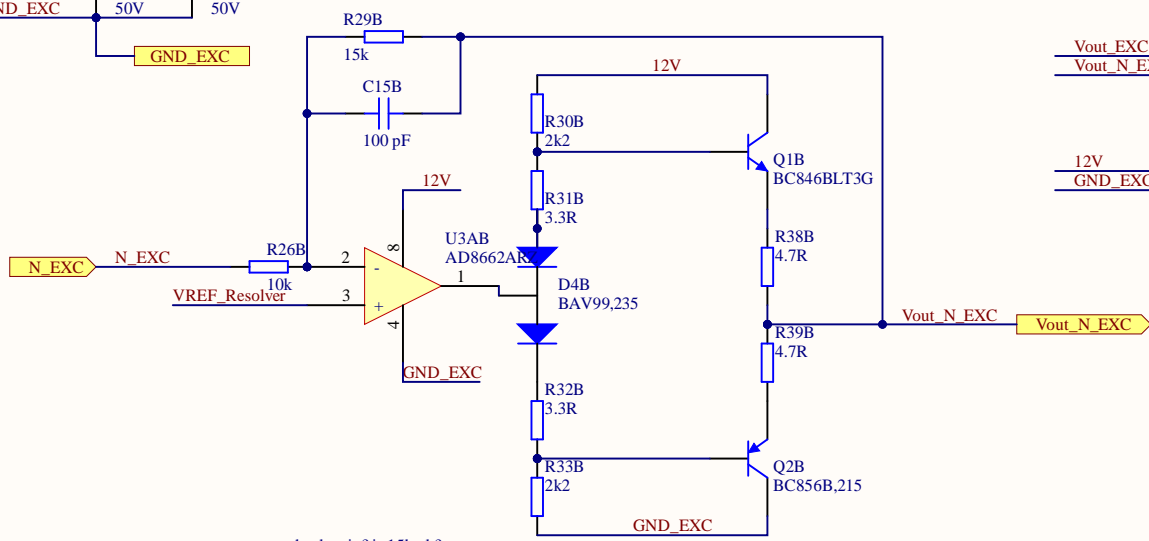
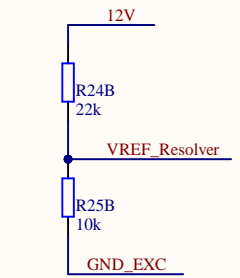


Title Buffer_EXC.SchDoc		UltraZohm www.ultrazohm.com	
Revision: Rev02	Design Engineer: Martin Bauer		
Project: UZ_D_Resolver.PjPCB		Date: 20.02.2023	
		Sheet 4.1.bf 14	



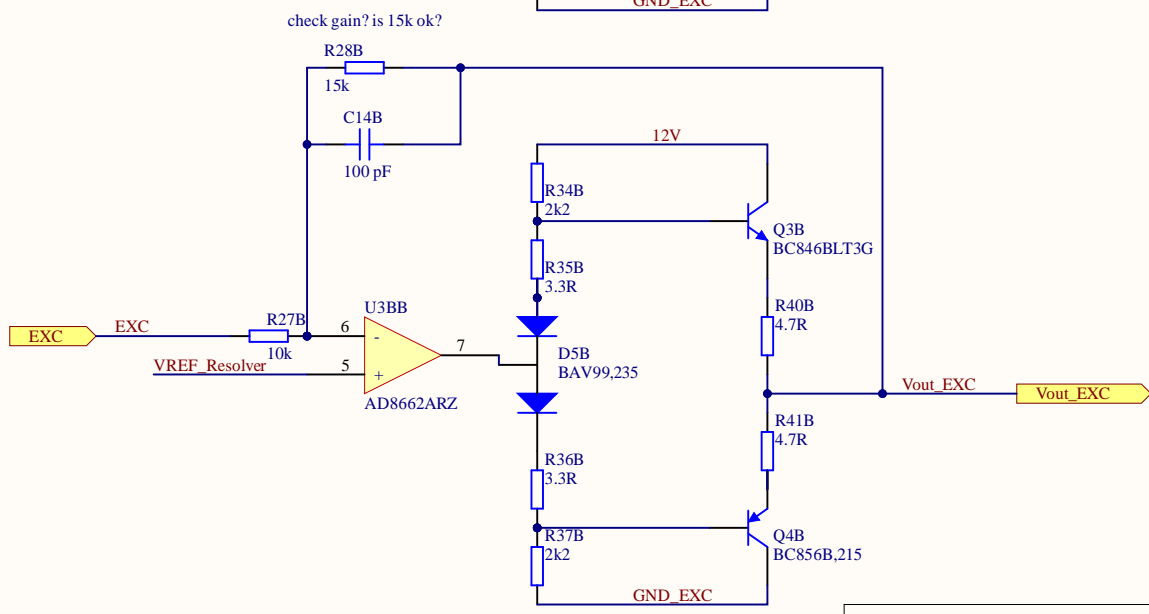
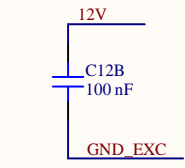
A

A



B

B




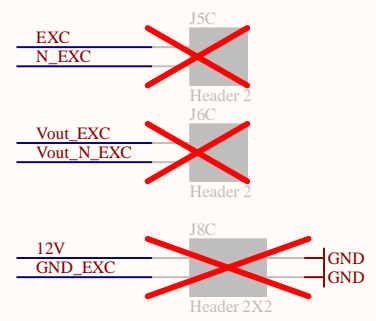
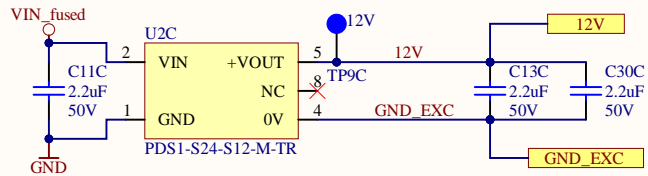
C

C

D

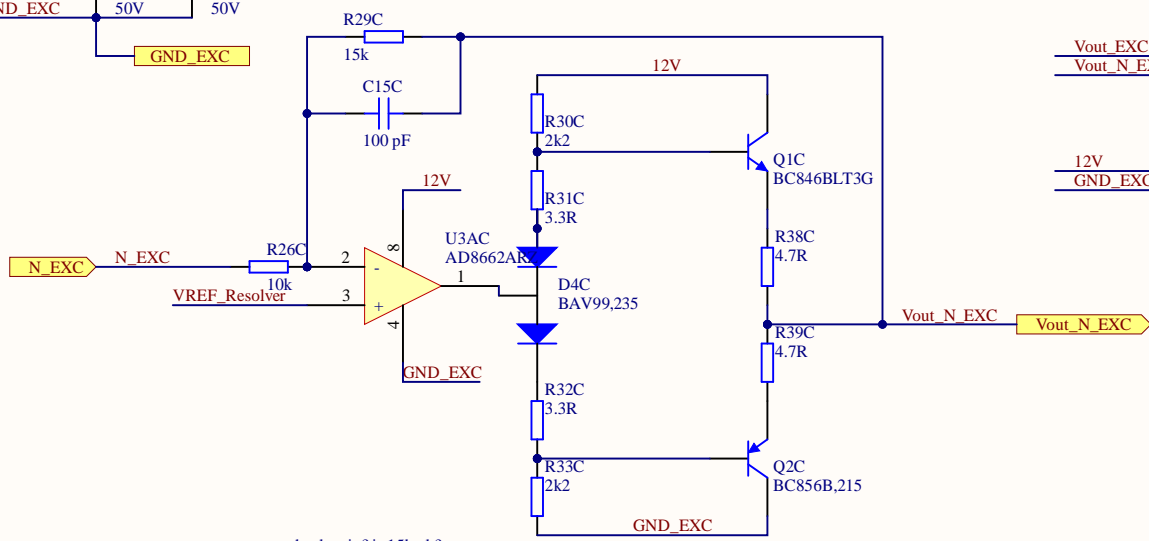
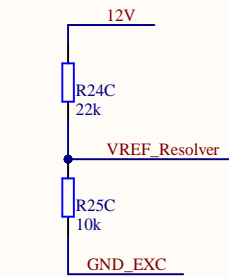
D

Title Buffer_EXC.SchDoc		
Revision: Rev02	Design Engineer: Martin Bauer	
Project: UZ_D_Resolver.PjPCB		
Date: 20.02.2023		Sheet 4.2.bf 14



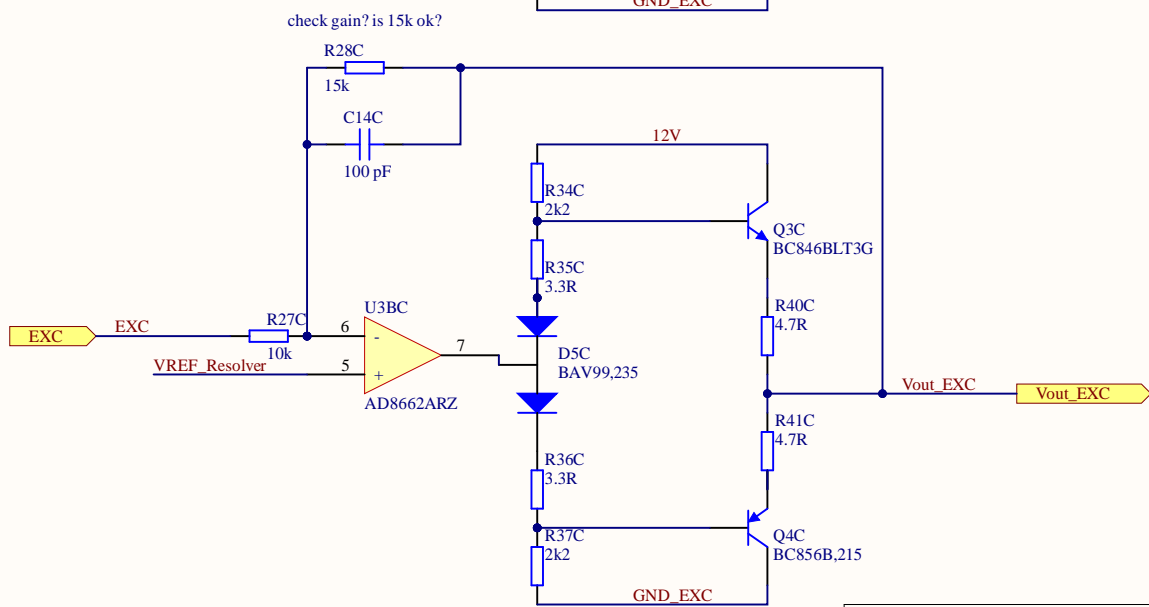
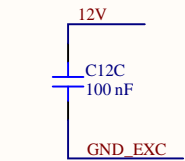
A

A



B

B



C

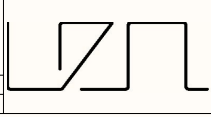
C

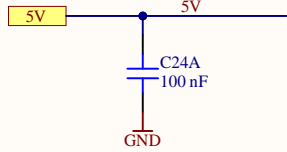
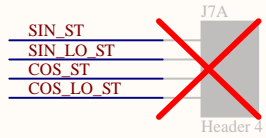
D

D

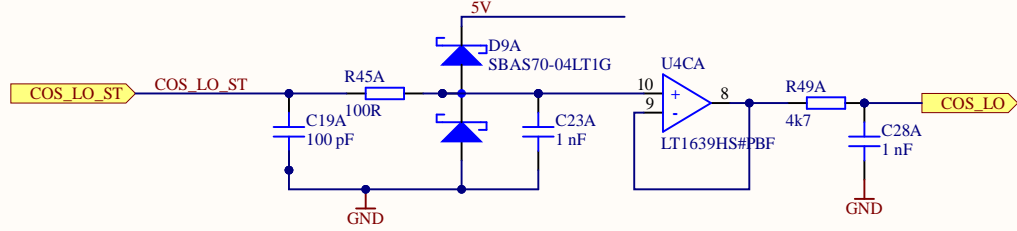
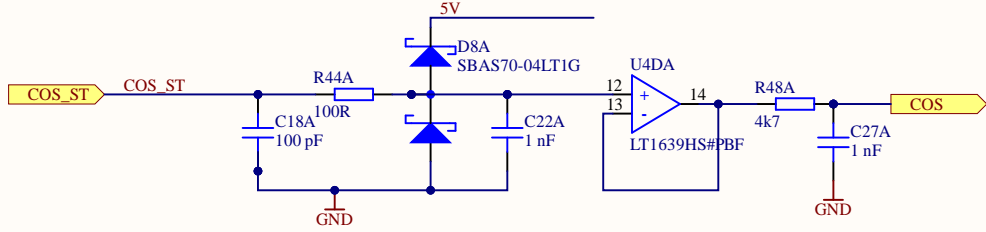
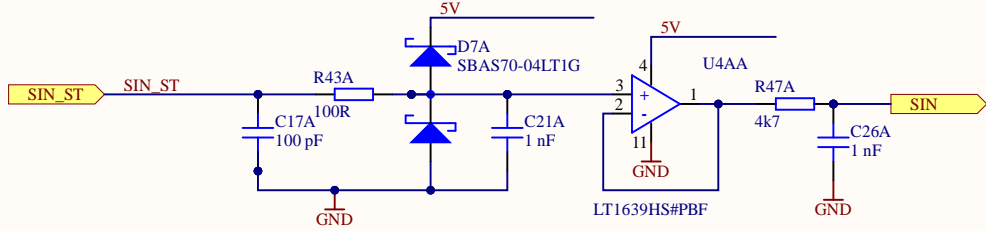
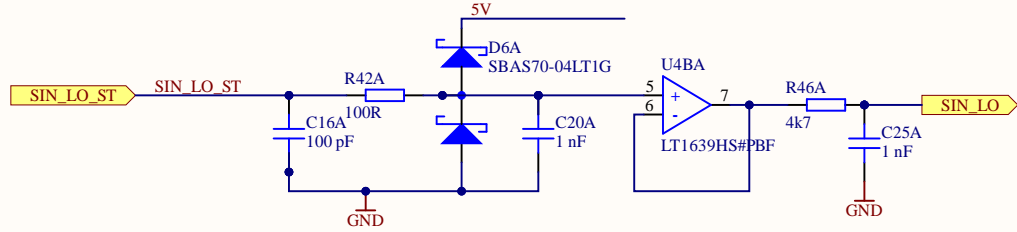
Title Buffer_EXC.SchDoc	
Revision: Rev02	Design Engineer: Martin Bauer
Project: UZ_D_Resolver.PjPCB	

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4x SBAS70-04LT1G



Title Impedance converter.SchDoc

Revision: Rev02 Design Engineer: Martin Bauer

Project: UZ_D_Resolver.PjPCB

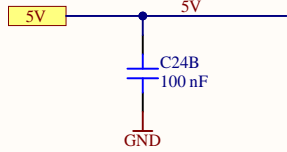
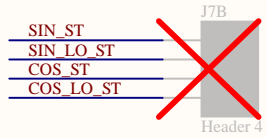
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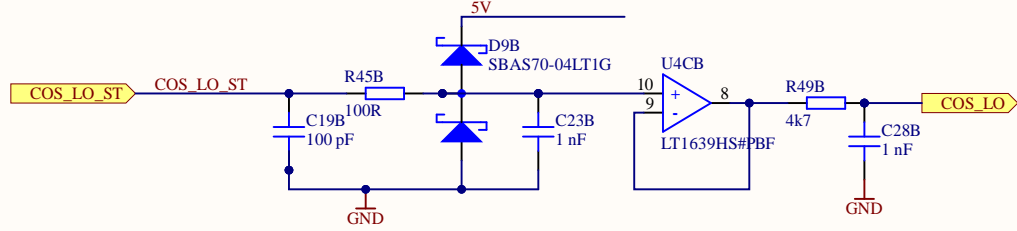
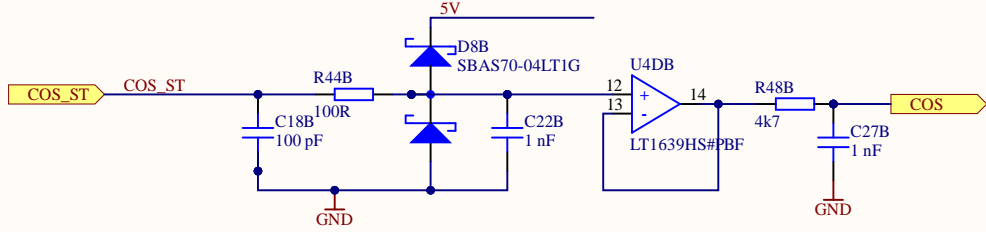
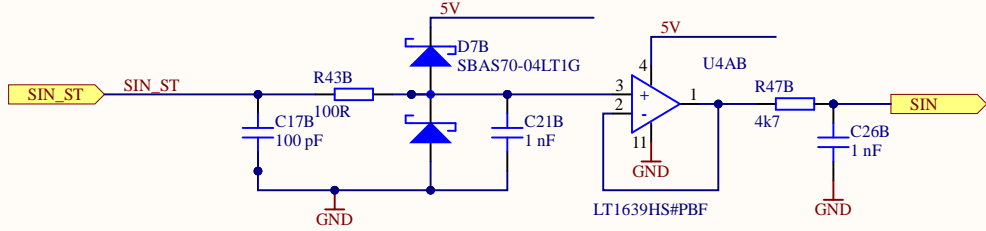
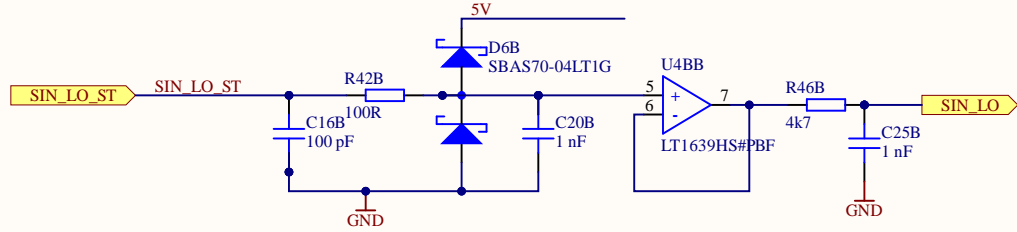
Date: 20.02.2023

Sheet 5.1.bf 14





4x SBAS70-04LT1G



Title Impedance converter.SchDoc

Revision: Rev02 Design Engineer: Martin Bauer

Project: UZ_D_Resolver.PjPCB

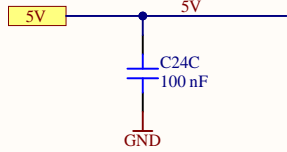
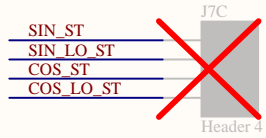
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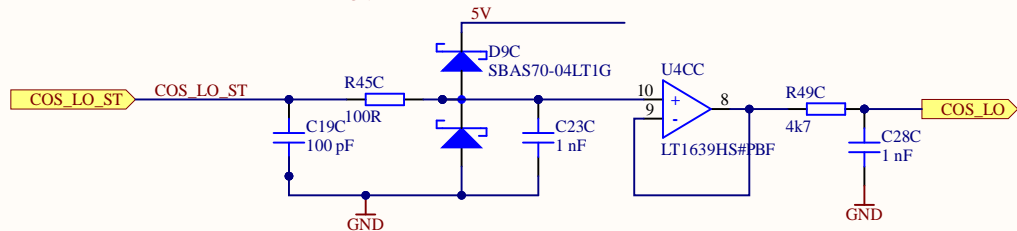
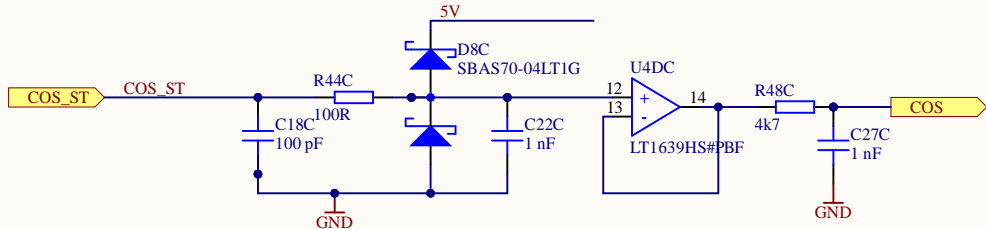
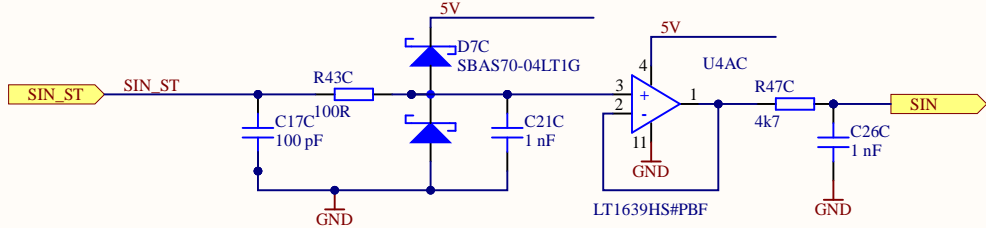
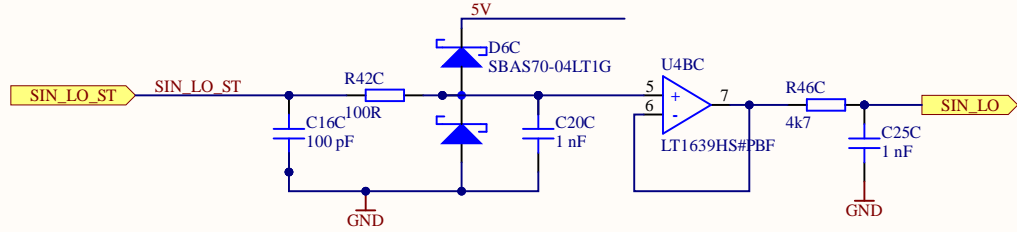
Date: 20.02.2023

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4x SBAS70-04LT1G



Title Impedance converter.SchDoc

Revision: Rev02 Design Engineer: Martin Bauer

Project: UZ_D_Resolver.PjPCB

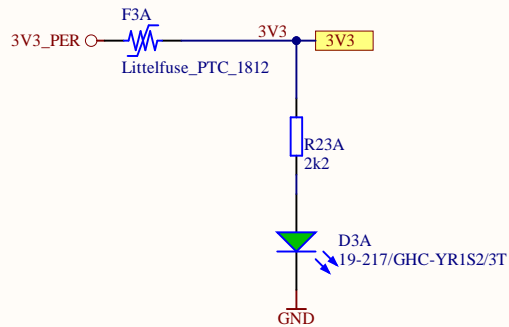
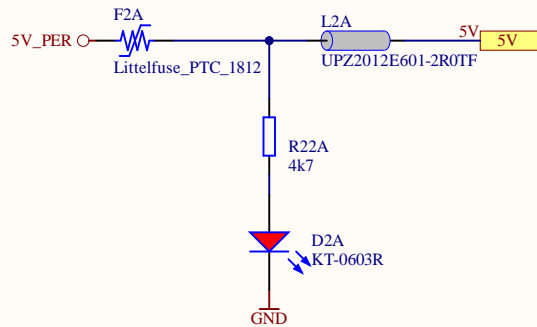
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Date: 20.02.2023

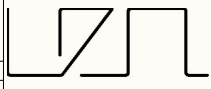
Sheet 5.3.bf 14

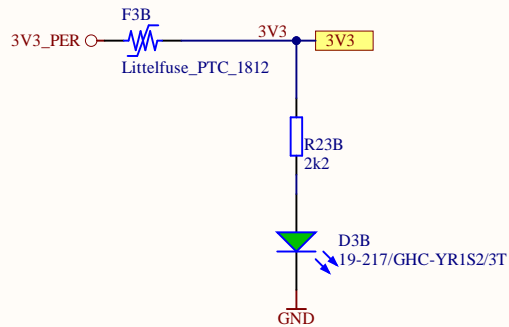
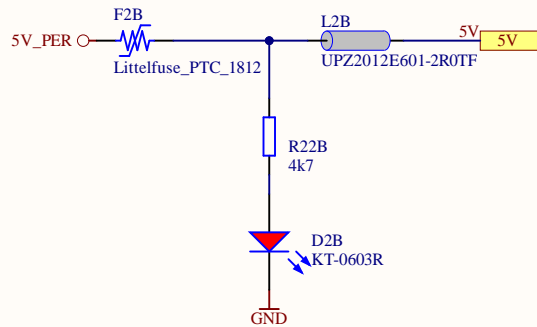




Title Resolver fuses.SchDoc	
Revision: Rev02	Design Engineer: Martin Bauer
Project: UZ_D_Resolver.PjPCB	

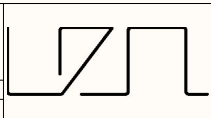
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Date: 20.02.2023
Sheet 6.1.bf 14

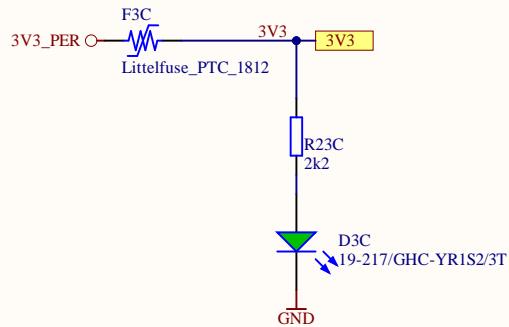
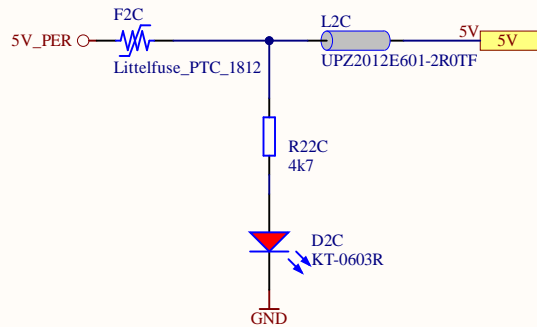




Title Resolver fuses.SchDoc	
Revision: Rev02	Design Engineer: Martin Bauer
Project: UZ_D_Resolver.PjPCB	

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Title Resolver fuses.SchDoc	
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