CarrierConnector
FPGA Connector.SchDoc

DAC_IN
CLK_P
CLK_N
CVN_P
CVN_N
DAC_IN_P[1..8]
DAC_IN_N[1..8]
PILOT_IN
PILOT_OUT
Collective_FLT

LVDS Receiver_Data
LVDS_Receiver_Data.SchDoc

DAC_IN DAC_IN_C[1..8]

LVDS Receiver_CVN_CLK
LVDS_Receiver_CVN_CLK.SchDoc

CLK_P
CLK_N
CVN_P
CVN_N
CLK[1..8]
CVN[1..8]

DAC_IN_C[1..8]
DAC_IN_C
CLK[1..8]
CVN[1..8]
CLK
CVN

REPEAT(DAC, 1, 8)
DAC.SchDoc

Repeat(D_IN) Repeat(OP_AMP_P)
Repeat(OP_AMP_N)
Repeat(OPAMP_FB)
Repeat(CLK)
Repeat(CVN)

OP_AMP_P
OP_AMP_N
OPAMP_FB

DAC_Reference
DAC_Reference.SchDoc

REPEAT(OpAmp,1,8)
OpAmp_Channnels.SchDoc

Repeat(OP_AMP_P)
Repeat(OP_AMP_N)
Repeat(OPAMP_FB)
Repeat(DIN_P)
Repeat(DIN_N)

DIN_P
DIN_N
DIN_P[1..8]
DIN_N[1..8]

U_AnalogConnector
Ethernet_Connector.SchDoc

DIN_P[1..8]
DIN_N[1..8]

DIN from analog card for HITL usage

Power_Pos
Power_Pos.SchDoc

Power_Neg
Power_Neg.SchDoc

LOGO1
UltraZohm
UZ Logo

Revision1

05/22

Serial
Serial1

UZ_A_DAC

Designer1

13.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you must decide how many levels to use in the stack. To reduce the TTL/CMOS to LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in Figure 22.

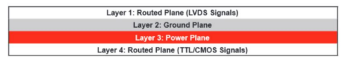

Figure 22. Four-Layer PCB Board

NOTE
The separation between layers 2 and 3 should be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

Title Top Sheet.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
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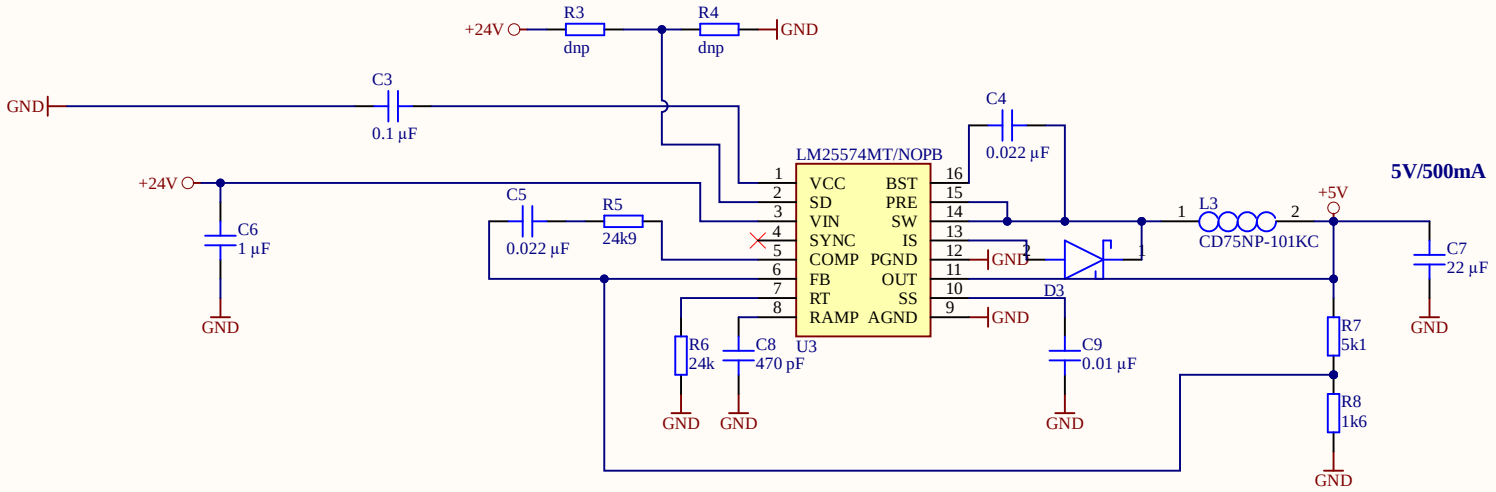
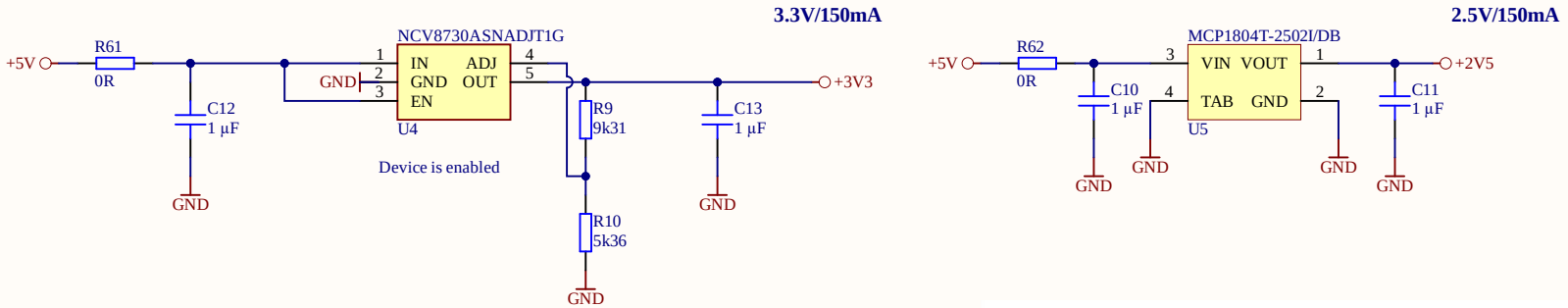
PSU: +5V, +3V3, +2V5, +1V8

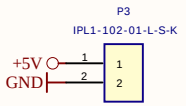
SYNC	Oscillator synchronization input or output The internal oscillator can be synchronized to an external clock with an external pull-down device. Multiple LM25574 devices can be synchronized together by connection of their SYNC pins.

a 5 µA pull-up current source configures the regulator fully operational.





EN	Enable input pin (high – enabled, low – disabled). If this pin is connected to IN pin or if it is left unconnected (pull–up resistor is not required) the device is enabled.
ADJ	Adjust input pin, could be connected to the resistor divider to the OUT pin.



Samtec Connector can be swapped for a regular Pin Header

the IC temperature falls this way, the LDO is back enabled. The thermal shutdown feature provides the protection against overheating due to some application failure and it is not intended to be used as a normal working function.

Power Dissipation

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum power dissipation is dependent on the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature. The maximum power dissipation can be computed by following equation:

$$P_{D(MAX)} = \frac{T_J - T_A}{\theta_{JA}} = \frac{125 - T_A}{\theta_{JA}} \text{ [W]} \quad \text{(eq. 27)}$$

Where: $(T_J - T_A)$ is the temperature difference between the junction and ambient temperatures and θ_{JA} is the thermal resistance (dependent on the PCB as mentioned above).

For reliable operation junction temperature should be less than +125°C.

The power dissipated by the LDO for given application conditions can be calculated by the next equation:

$$P_D = V_{IN} \cdot I_{GND} + (V_{IN} - V_{OUT}) \cdot I_{OUT} \text{ [W]} \quad \text{(eq. 28)}$$

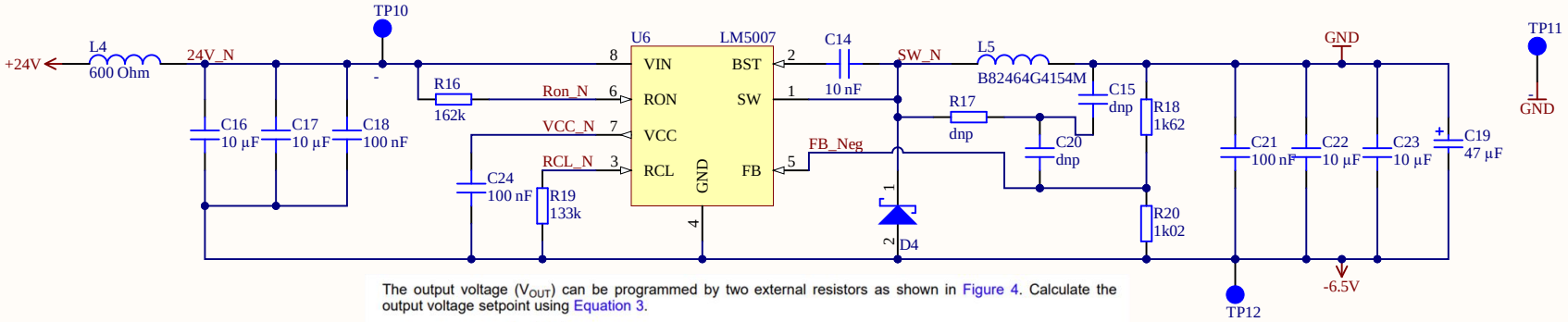
Where: I_{GND} is the LDO's ground current, dependent on the output load current.

Connecting the exposed pad and NC pin to a large ground planes helps to dissipate the heat from the chip.

The relation of θ_{JA} and $P_{D(MAX)}$ to PCB copper area and Cu layer thickness could be seen on the Figures 68 and 69.

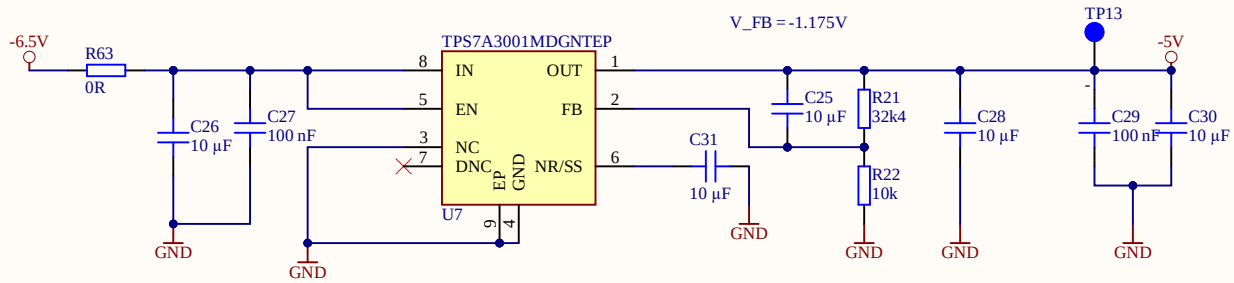
PSU: -6.28V, -5V, negRail

DNC	7	**DO NOT CONNECT**. Do not route this pin to any electrical net, not even GND or IN.



The output voltage (V_{OUT}) can be programmed by two external resistors as shown in Figure 4. Calculate the output voltage setpoint using Equation 3.

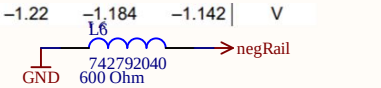
$$V_{OUT} = 2.5\,V \cdot \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$



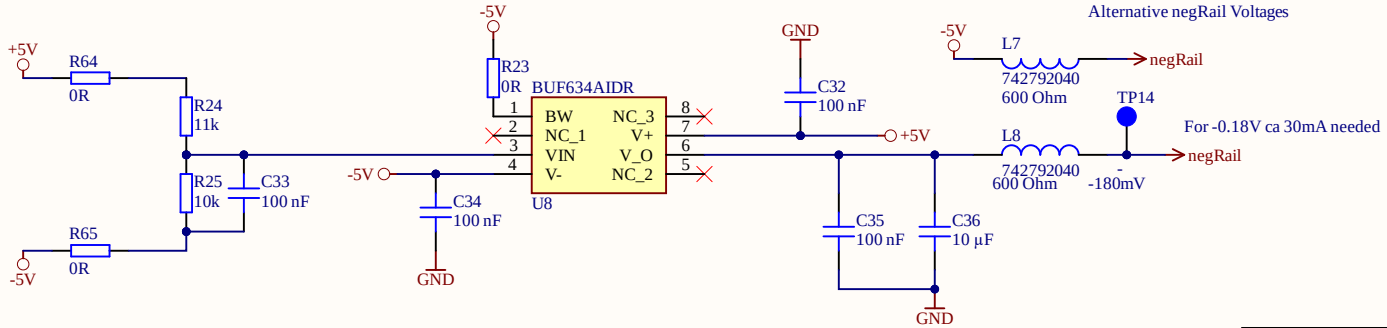
-5V/-200mA

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}} - 1\right), \quad \text{where } \frac{V_{OUT}}{R_1 + R_2} \geq 5\mu A$$

V_{REF}	Internal reference	$V_{NR/SS} = V_{REF}$	−1.22	−1.184	−1.142	V



Alternative negRail Voltages

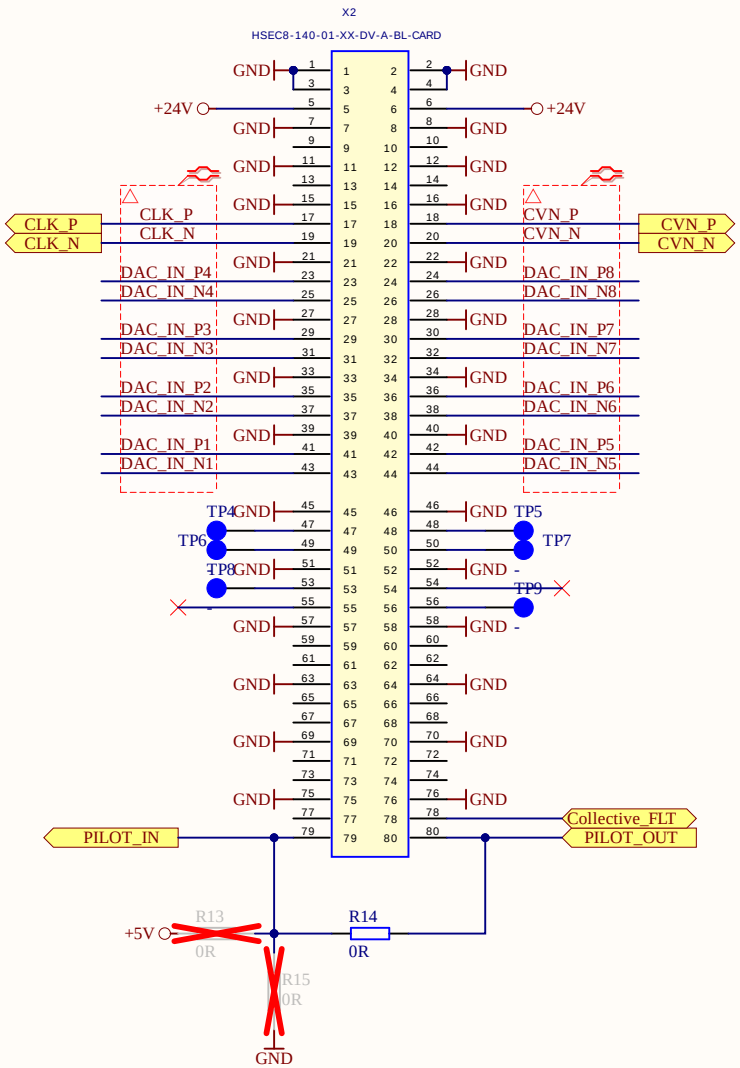


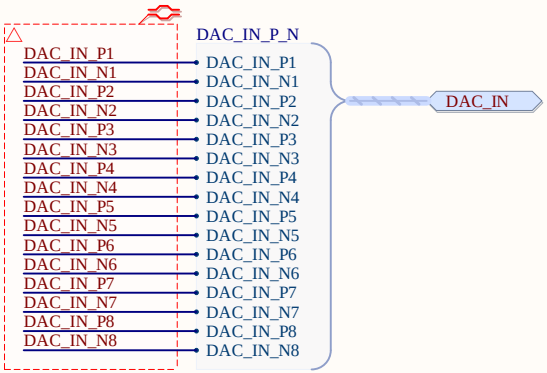
NC=No internal connection

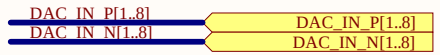
Zweck BUF634:
Workaround: Verwendung als open-loop Verstärker,
kleine negative Spannung um das negative Rail des differentiellen OpAmps THS4521 zu versorgen, s. Kapitel 11 Datenblatt THS4561. --> rail-to-rail

Title Power_Neg.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 3 of 24

UltraZohm Connector

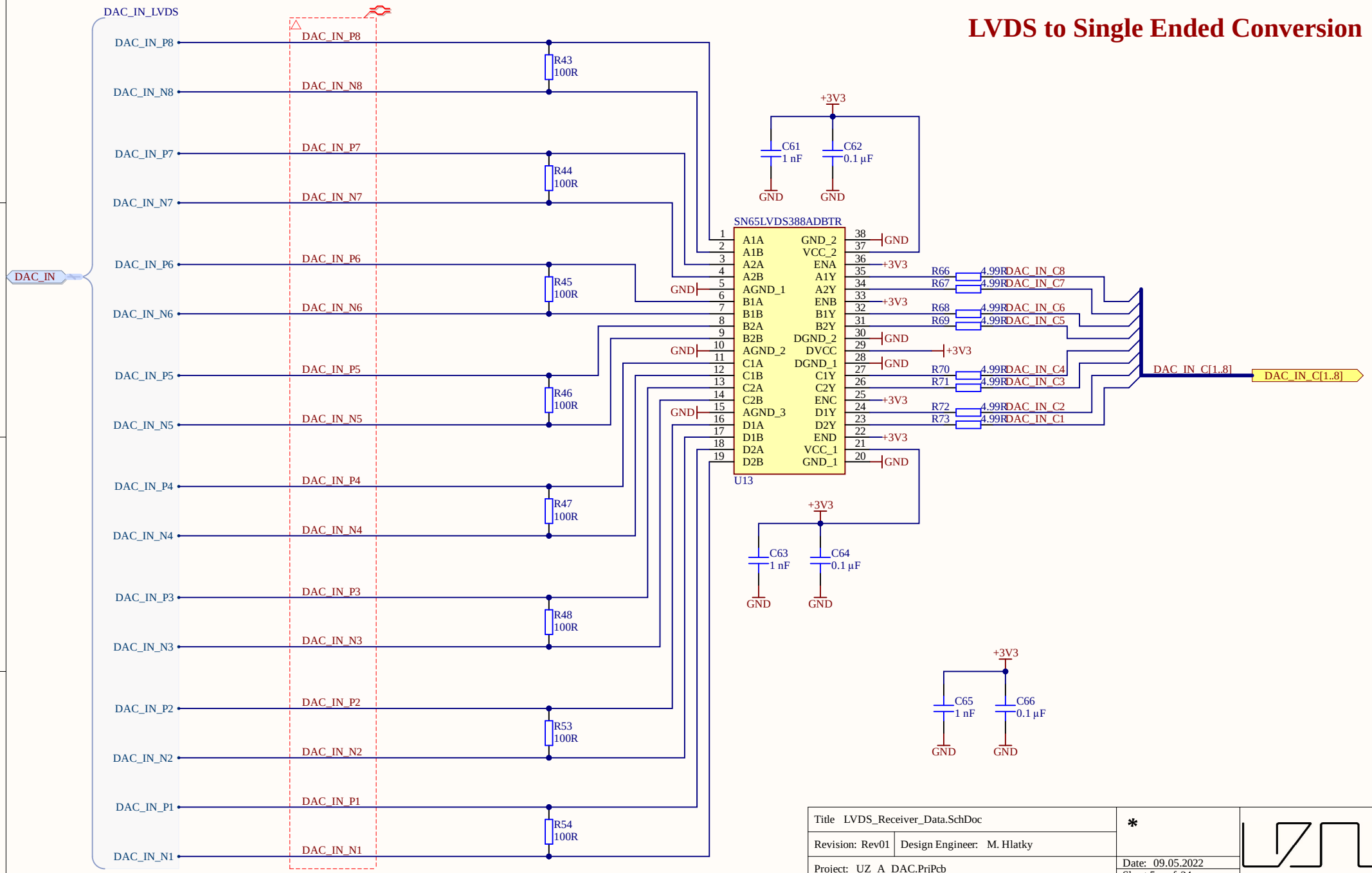






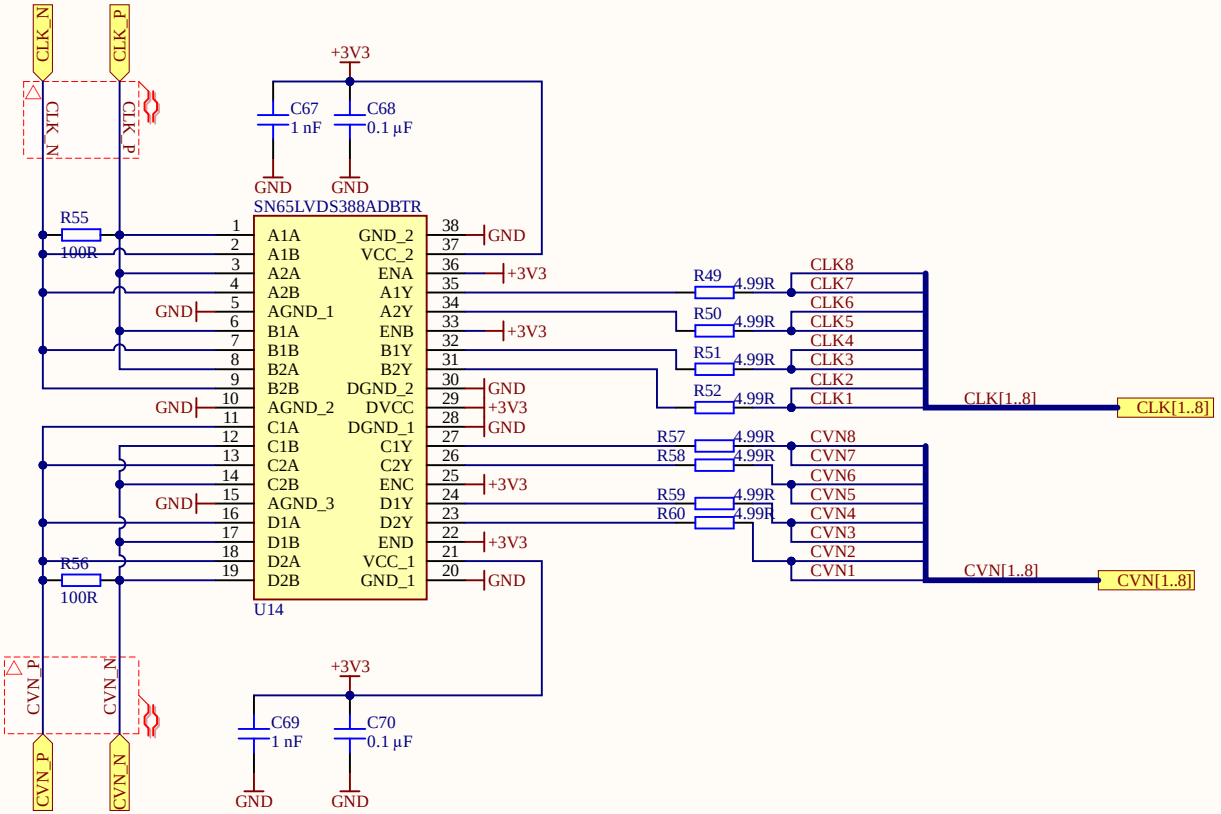
Title FPGA Connector.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 4 of 24

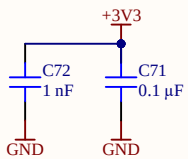
LVDS to Single Ended Conversion

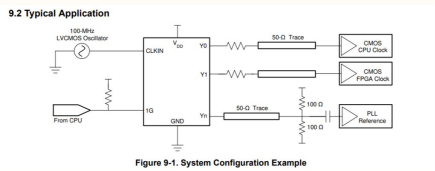


Title LVDS_Receiver_Data.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 5 of 24

Conversion and Clock Signal Distribution







Title LVDS_Receiver_CVN_CLK.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 6 of 24

DAC 1-8

OUTPUT RANGE

The output of the DAC is

$V_{OUT} = (V_{REF} \times Code)/65536.$

Where *Code* is the decimal data word loaded to the DAC latch.

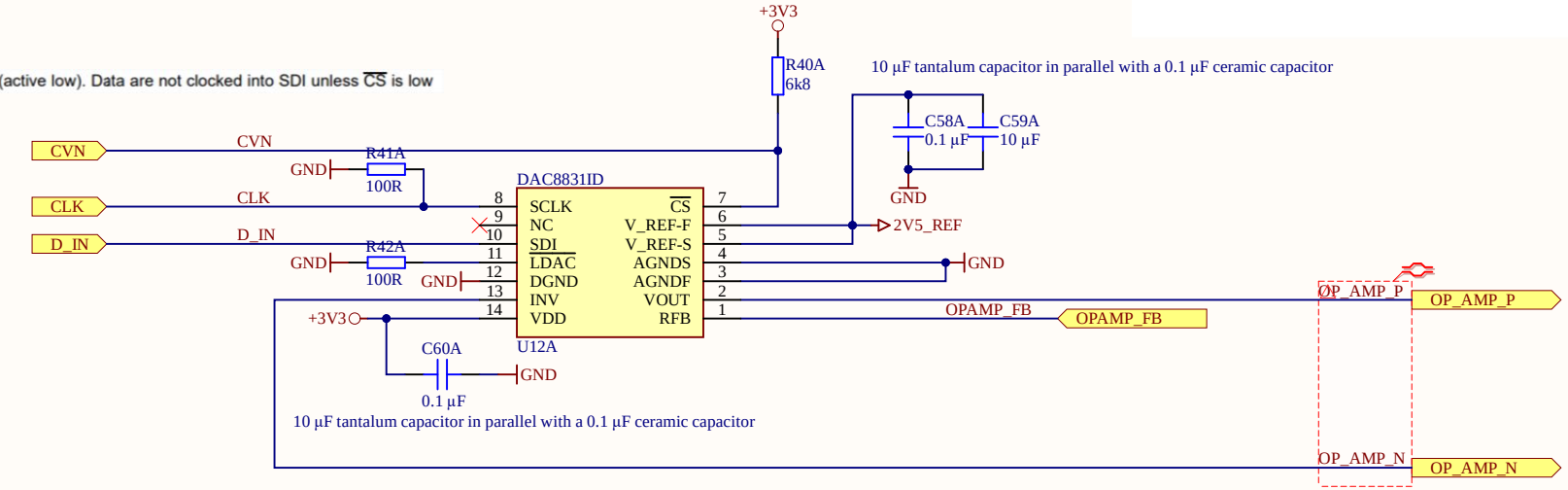
Serial Interface

The digital interface is a standard 3-wire connection compatible with SPI, QSPI™, Microwire™, and TI DSP interfaces, which can operate at speeds up to 50 M-bits/sec. The data transfer is framed by $\overline{CS}$, the chip select signal. The DAC works as a bus slave. The bus master generates the synchronize clock, SCLK, and initiates the transmission. When $\overline{CS}$ is high, the DAC is not accessed, and the clock SCLK and serial input data SDI are ignored. The bus master accesses the DAC by driving pin $\overline{CS}$ low. Immediately following the high-to-low transition of $\overline{CS}$, the serial input data on pin SDI is shifted out from the bus master synchronously on the falling edge of SCLK, and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of $\overline{CS}$ transfers the contents of the input shift register to the input register. All data registers are 16-bit. It takes 16 clocks of SCLK to transfer one data word to the parts. To complete a whole data word, $\overline{CS}$ must go high immediately after 16 SCLKs are clocked in. If more than 16 SCLKs are applied during the low state of $\overline{CS}$, the last 16 bits are transferred to the input register on the rising edge of $\overline{CS}$. However, if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data is corrupted. In this case, reload the DAC with a new 16-bit word.

In the DAC8830, the contents of the input register are transferred into the DAC latch immediately when the input register is loaded, and the DAC output is updated at the same time.

The DAC8831 has an $\overline{LDAC}$ pin allowing the DAC latch to be updated asynchronously by bringing $\overline{LDAC}$ low after $\overline{CS}$ goes high. In this case, $\overline{LDAC}$ must be maintained high while $\overline{CS}$ is low. If $\overline{LDAC}$ is tied permanently low, the DAC latch is updated immediately after the input register is loaded (caused by the low-to-high transition of $\overline{CS}$).

$\overline{CS}$ | Chip select input (active low). Data are not clocked into SDI unless $\overline{CS}$ is low



10 SDI | Serial data input. Data are latched into input register on the rising edge of SCLK.

$\overline{LDAC}$ | Load DAC control input. Active low. When $\overline{LDAC}$ is Low, the DAC latch is simultaneously updated with the content of the input register.

NC | No internal connection

Title DAC.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 7.1 of 24

DAC 1-8

OUTPUT RANGE

The output of the DAC is

$V_{OUT} = (V_{REF} \times Code)/65536.$

Where *Code* is the decimal data word loaded to the DAC latch.

Serial Interface

The digital interface is a standard 3-wire connection compatible with SPI, QSPI™, Microwire™, and TI DSP interfaces, which can operate at speeds up to 50 M-bits/sec. The data transfer is framed by $\overline{CS}$, the chip select signal. The DAC works as a bus slave. The bus master generates the synchronize clock, SCLK, and initiates the transmission. When $\overline{CS}$ is high, the DAC is not accessed, and the clock SCLK and serial input data SDI are ignored. The bus master accesses the DAC by driving pin $\overline{CS}$ low. Immediately following the high-to-low transition of $\overline{CS}$, the serial input data on pin SDI is shifted out from the bus master synchronously on the falling edge of SCLK, and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of $\overline{CS}$ transfers the contents of the input shift register to the input register. All data registers are 16-bit. It takes 16 clocks of SCLK to transfer one data word to the parts. To complete a whole data word, $\overline{CS}$ must go high immediately after 16 SCLKs are clocked in. If more than 16 SCLKs are applied during the low state of $\overline{CS}$, the last 16 bits are transferred to the input register on the rising edge of $\overline{CS}$. However, if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data is corrupted. In this case, reload the DAC with a new 16-bit word.

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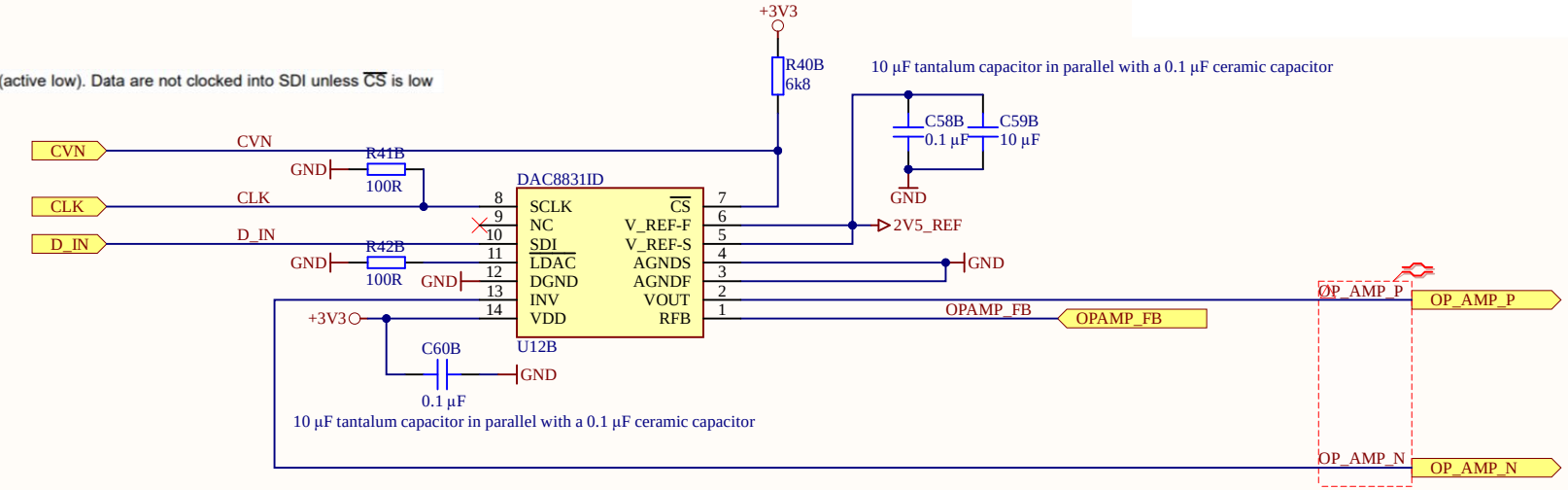

$\overline{CS}$		Chip select input (active low). Data are not clocked into SDI unless $\overline{CS}$ is low
10	SDI	Serial data input. Data are latched into input register on the rising edge of SCLK.
	$\overline{LDAC}$	Load DAC control input. Active low. When $\overline{LDAC}$ is Low, the DAC latch is simultaneously updated with the content of the input register.

NC	No internal connection

Title DAC.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 7.2 of 24

DAC 1-8

OUTPUT RANGE

The output of the DAC is

$V_{OUT} = (V_{REF} \times Code)/65536.$

Where *Code* is the decimal data word loaded to the DAC latch.

Serial Interface

The digital interface is a standard 3-wire connection compatible with SPI, QSPI™, Microwire™, and TI DSP interfaces, which can operate at speeds up to 50 M-bits/sec. The data transfer is framed by $\overline{CS}$, the chip select signal. The DAC works as a bus slave. The bus master generates the synchronize clock, SCLK, and initiates the transmission. When $\overline{CS}$ is high, the DAC is not accessed, and the clock SCLK and serial input data SDI are ignored. The bus master accesses the DAC by driving pin $\overline{CS}$ low. Immediately following the high-to-low transition of $\overline{CS}$, the serial input data on pin SDI is shifted out from the bus master synchronously on the falling edge of SCLK, and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of $\overline{CS}$ transfers the contents of the input shift register to the input register. All data registers are 16-bit. It takes 16 clocks of SCLK to transfer one data word to the parts. To complete a whole data word, $\overline{CS}$ must go high immediately after 16 SCLKs are clocked in. If more than 16 SCLKs are applied during the low state of $\overline{CS}$, the last 16 bits are transferred to the input register on the rising edge of $\overline{CS}$. However, if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data is corrupted. In this case, reload the DAC with a new 16-bit word.

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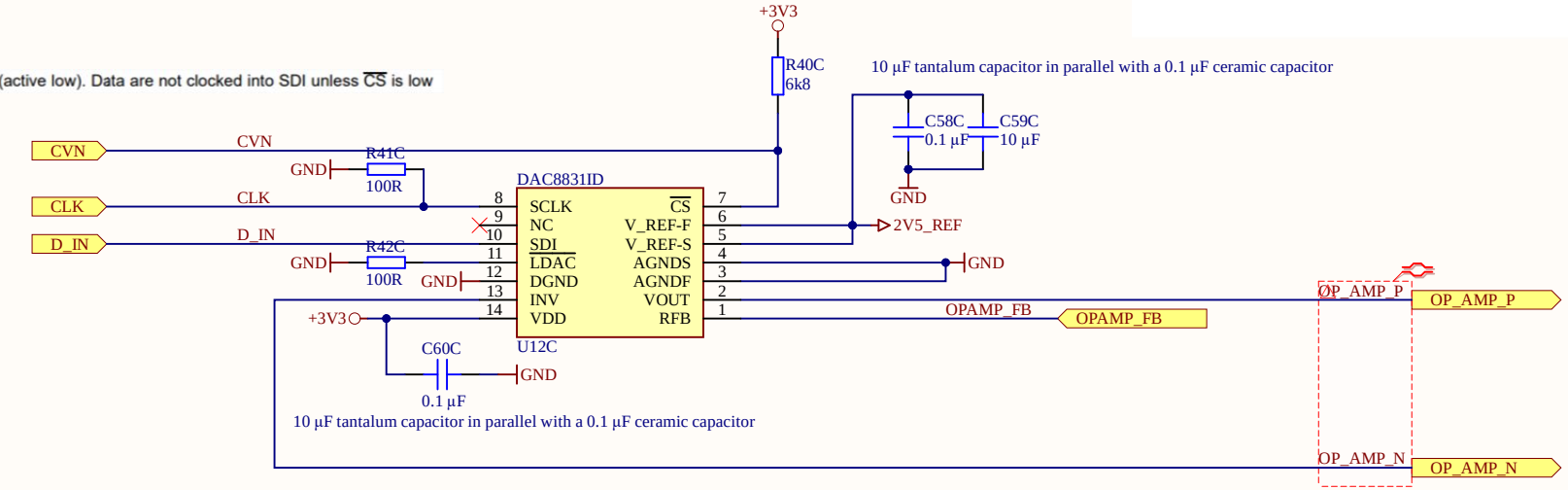
$\overline{CS}$ | Chip select input (active low). Data are not clocked into SDI unless $\overline{CS}$ is low



10 SDI | Serial data input. Data are latched into input register on the rising edge of SCLK.

$\overline{LDAC}$ | Load DAC control input. Active low. When $\overline{LDAC}$ is Low, the DAC latch is simultaneously updated with the content of the input register.

NC | No internal connection

Title DAC.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 7.3 of 24

DAC 1-8

OUTPUT RANGE

The output of the DAC is

$V_{OUT} = (V_{REF} \times Code)/65536.$

Where *Code* is the decimal data word loaded to the DAC latch.

Serial Interface

The digital interface is a standard 3-wire connection compatible with SPI, QSPI™, Microwire™, and TI DSP interfaces, which can operate at speeds up to 50 M-bits/sec. The data transfer is framed by $\overline{CS}$, the chip select signal. The DAC works as a bus slave. The bus master generates the synchronize clock, SCLK, and initiates the transmission. When $\overline{CS}$ is high, the DAC is not accessed, and the clock SCLK and serial input data SDI are ignored. The bus master accesses the DAC by driving pin $\overline{CS}$ low. Immediately following the high-to-low transition of $\overline{CS}$, the serial input data on pin SDI is shifted out from the bus master synchronously on the falling edge of SCLK, and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of $\overline{CS}$ transfers the contents of the input shift register to the input register. All data registers are 16-bit. It takes 16 clocks of SCLK to transfer one data word to the parts. To complete a whole data word, $\overline{CS}$ must go high immediately after 16 SCLKs are clocked in. If more than 16 SCLKs are applied during the low state of $\overline{CS}$, the last 16 bits are transferred to the input register on the rising edge of $\overline{CS}$. However, if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data is corrupted. In this case, reload the DAC with a new 16-bit word.

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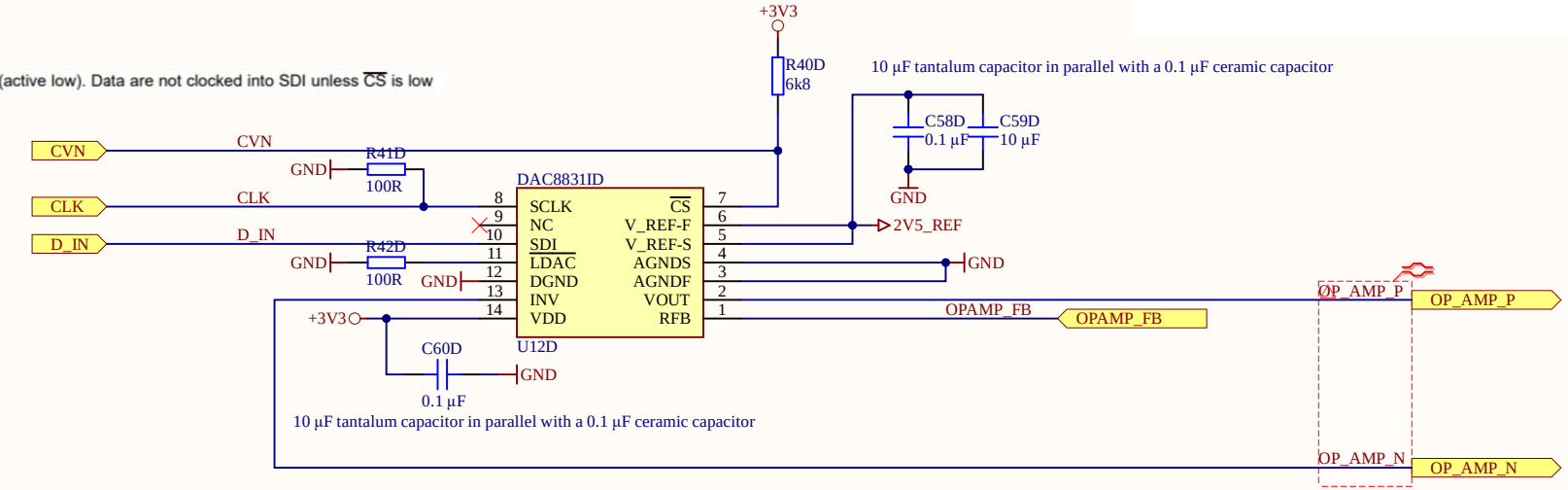
$\overline{CS}$ | Chip select input (active low). Data are not clocked into SDI unless $\overline{CS}$ is low



10 SDI | Serial data input. Data are latched into input register on the rising edge of SCLK.

$\overline{LDAC}$ | Load DAC control input. Active low. When $\overline{LDAC}$ is Low, the DAC latch is simultaneously updated with the content of the input register.

NC | No internal connection

Title DAC.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
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DAC 1-8

OUTPUT RANGE

The output of the DAC is

$$V_{OUT} = (V_{REF} \times Code)/65536.$$

Where *Code* is the decimal data word loaded to the DAC latch.

Serial Interface

The digital interface is a standard 3-wire connection compatible with SPI, QSPI™, Microwire™, and TI DSP interfaces, which can operate at speeds up to 50 M-bits/sec. The data transfer is framed by $\overline{CS}$, the chip select signal. The DAC works as a bus slave. The bus master generates the synchronize clock, SCLK, and initiates the transmission. When $\overline{CS}$ is high, the DAC is not accessed, and the clock SCLK and serial input data SDI are ignored. The bus master accesses the DAC by driving pin $\overline{CS}$ low. Immediately following the high-to-low transition of $\overline{CS}$, the serial input data on pin SDI is shifted out from the bus master synchronously on the falling edge of SCLK, and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of $\overline{CS}$ transfers the contents of the input shift register to the input register. All data registers are 16-bit. It takes 16 clocks of SCLK to transfer one data word to the parts. To complete a whole data word, $\overline{CS}$ must go high immediately after 16 SCLKs are clocked in. If more than 16 SCLKs are applied during the low state of $\overline{CS}$, the last 16 bits are transferred to the input register on the rising edge of $\overline{CS}$. However, if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data is corrupted. In this case, reload the DAC with a new 16-bit word.

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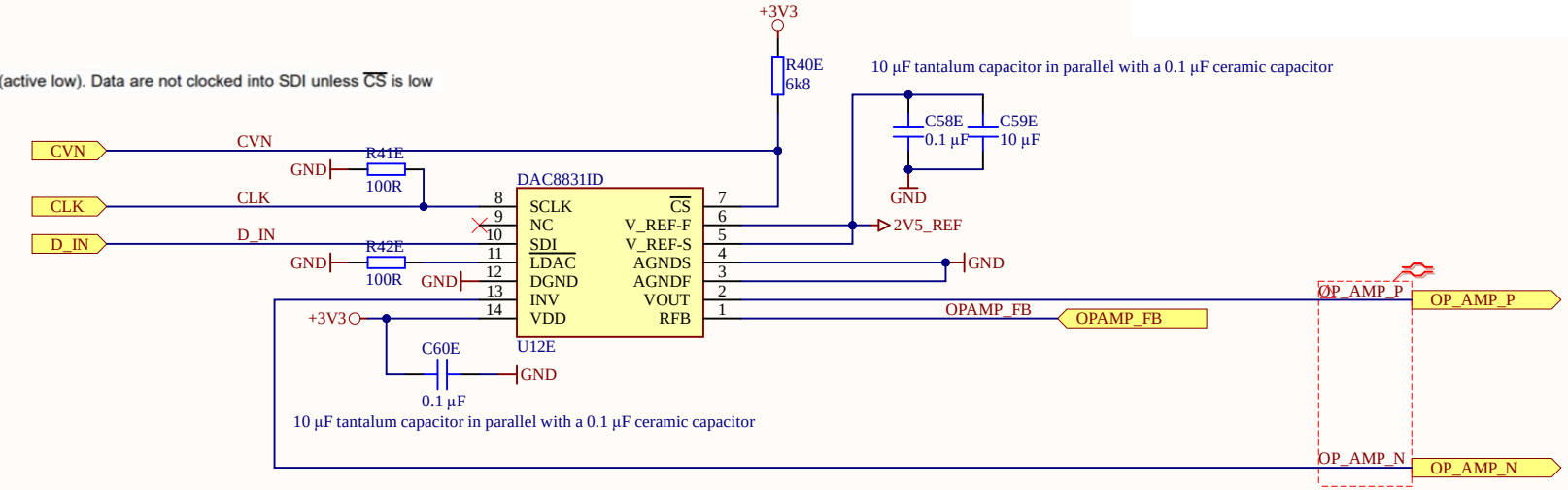
$\overline{CS}$ | Chip select input (active low). Data are not clocked into SDI unless $\overline{CS}$ is low



10 SDI | Serial data input. Data are latched into input register on the rising edge of SCLK.

$\overline{LDAC}$ | Load DAC control input. Active low. When $\overline{LDAC}$ is Low, the DAC latch is simultaneously updated with the content of the input register.

NC | No internal connection

Title DAC.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 7.5 of 24

DAC 1-8

OUTPUT RANGE

The output of the DAC is

$V_{OUT} = (V_{REF} \times Code)/65536.$

Where *Code* is the decimal data word loaded to the DAC latch.

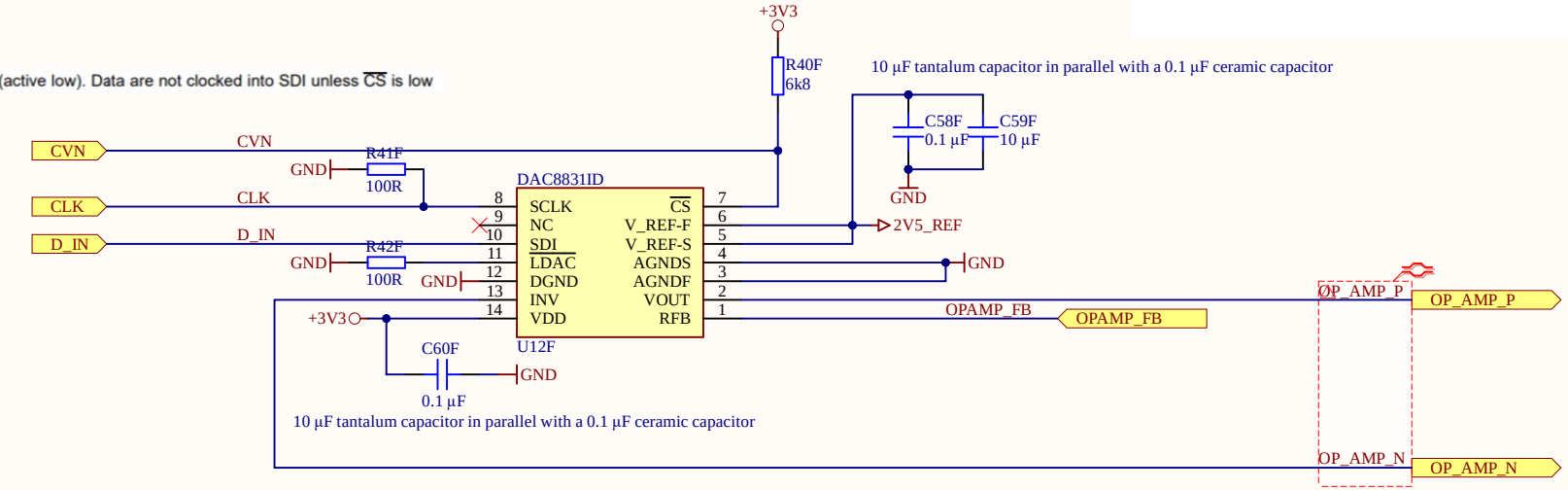
Serial Interface

The digital interface is a standard 3-wire connection compatible with SPI, QSPI™, Microwire™, and TI DSP interfaces, which can operate at speeds up to 50 M-bits/sec. The data transfer is framed by $\overline{CS}$, the chip select signal. The DAC works as a bus slave. The bus master generates the synchronize clock, SCLK, and initiates the transmission. When $\overline{CS}$ is high, the DAC is not accessed, and the clock SCLK and serial input data SDI are ignored. The bus master accesses the DAC by driving pin $\overline{CS}$ low. Immediately following the high-to-low transition of $\overline{CS}$, the serial input data on pin SDI is shifted out from the bus master synchronously on the falling edge of SCLK, and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of $\overline{CS}$ transfers the contents of the input shift register to the input register. All data registers are 16-bit. It takes 16 clocks of SCLK to transfer one data word to the parts. To complete a whole data word, $\overline{CS}$ must go high immediately after 16 SCLKs are clocked in. If more than 16 SCLKs are applied during the low state of $\overline{CS}$, the last 16 bits are transferred to the input register on the rising edge of $\overline{CS}$. However, if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data is corrupted. In this case, reload the DAC with a new 16-bit word.

In the DAC8830, the contents of the input register are transferred into the DAC latch immediately when the input register is loaded, and the DAC output is updated at the same time.

The DAC8831 has an $\overline{LDAC}$ pin allowing the DAC latch to be updated asynchronously by bringing $\overline{LDAC}$ low after $\overline{CS}$ goes high. In this case, $\overline{LDAC}$ must be maintained high while $\overline{CS}$ is low. If $\overline{LDAC}$ is tied permanently low, the DAC latch is updated immediately after the input register is loaded (caused by the low-to-high transition of $\overline{CS}$).

$\overline{CS}$ | Chip select input (active low). Data are not clocked into SDI unless $\overline{CS}$ is low



10 SDI | Serial data input. Data are latched into input register on the rising edge of SCLK.

$\overline{LDAC}$ | Load DAC control input. Active low. When $\overline{LDAC}$ is Low, the DAC latch is simultaneously updated with the content of the input register.

NC | No internal connection

Title DAC.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 7.6 of 24

DAC 1-8

OUTPUT RANGE

The output of the DAC is

$$V_{OUT} = (V_{REF} \times Code)/65536.$$

Where *Code* is the decimal data word loaded to the DAC latch.

Serial Interface

The digital interface is a standard 3-wire connection compatible with SPI, QSPI™, Microwire™, and TI DSP interfaces, which can operate at speeds up to 50 M-bits/sec. The data transfer is framed by $\overline{CS}$, the chip select signal. The DAC works as a bus slave. The bus master generates the synchronize clock, SCLK, and initiates the transmission. When $\overline{CS}$ is high, the DAC is not accessed, and the clock SCLK and serial input data SDI are ignored. The bus master accesses the DAC by driving pin $\overline{CS}$ low. Immediately following the high-to-low transition of $\overline{CS}$, the serial input data on pin SDI is shifted out from the bus master synchronously on the falling edge of SCLK, and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of $\overline{CS}$ transfers the contents of the input shift register to the input register. All data registers are 16-bit. It takes 16 clocks of SCLK to transfer one data word to the parts. To complete a whole data word, $\overline{CS}$ must go high immediately after 16 SCLKs are clocked in. If more than 16 SCLKs are applied during the low state of $\overline{CS}$, the last 16 bits are transferred to the input register on the rising edge of $\overline{CS}$. However, if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data is corrupted. In this case, reload the DAC with a new 16-bit word.

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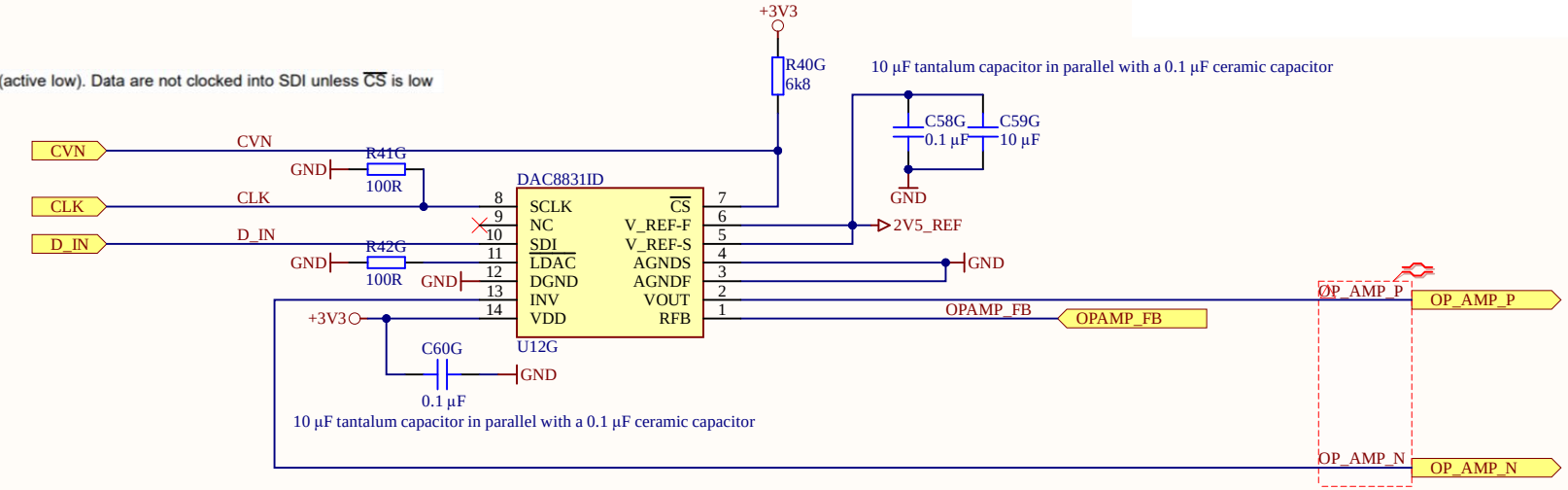

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Title DAC.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 7.7 of 24

DAC 1-8

OUTPUT RANGE

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Where *Code* is the decimal data word loaded to the DAC latch.

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The digital interface is a standard 3-wire connection compatible with SPI, QSPI™, Microwire™, and TI DSP interfaces, which can operate at speeds up to 50 M-bits/sec. The data transfer is framed by $\overline{CS}$, the chip select signal. The DAC works as a bus slave. The bus master generates the synchronize clock, SCLK, and initiates the transmission. When $\overline{CS}$ is high, the DAC is not accessed, and the clock SCLK and serial input data SDI are ignored. The bus master accesses the DAC by driving pin $\overline{CS}$ low. Immediately following the high-to-low transition of $\overline{CS}$, the serial input data on pin SDI is shifted out from the bus master synchronously on the falling edge of SCLK, and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of $\overline{CS}$ transfers the contents of the input shift register to the input register. All data registers are 16-bit. It takes 16 clocks of SCLK to transfer one data word to the parts. To complete a whole data word, $\overline{CS}$ must go high immediately after 16 SCLKs are clocked in. If more than 16 SCLKs are applied during the low state of $\overline{CS}$, the last 16 bits are transferred to the input register on the rising edge of $\overline{CS}$. However, if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data is corrupted. In this case, reload the DAC with a new 16-bit word.

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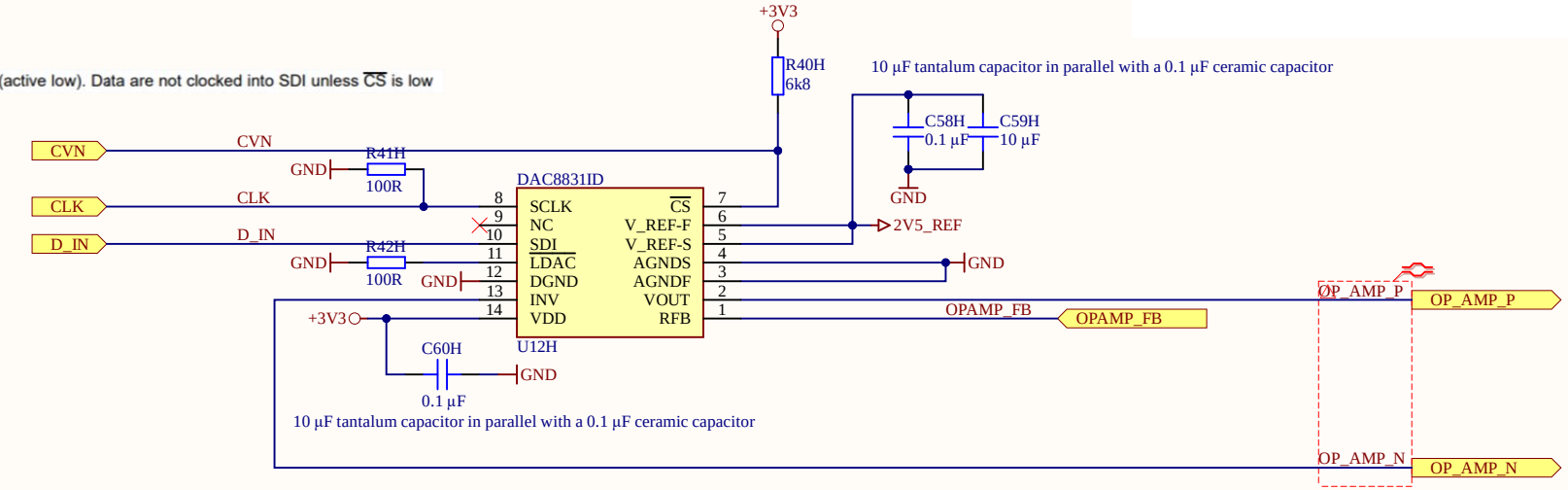

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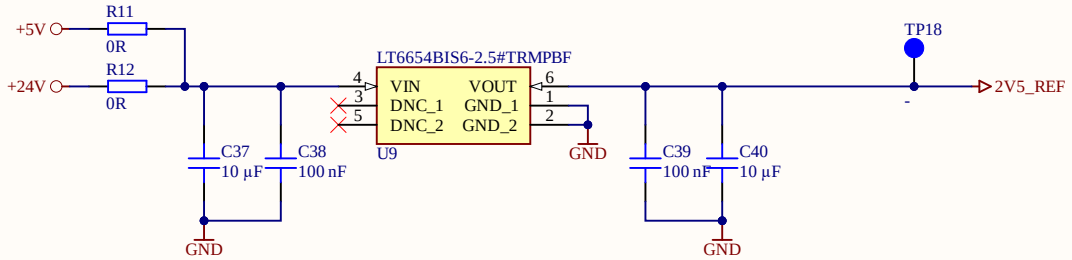
Title DAC.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 7.8 of 24

DAC Reference



LT6654 is available in 1.25V/2.048V/2.5V/3V/3.3V/4.096V/5V
For DAC

same as Pin 5

DNC (Pin 3): Do Not Connect. Keep leakage current from this pin to V_{IN} or GND to a minimum.

Title DAC_Reference.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 8 of 24

OP & Differential AMPs 1-8

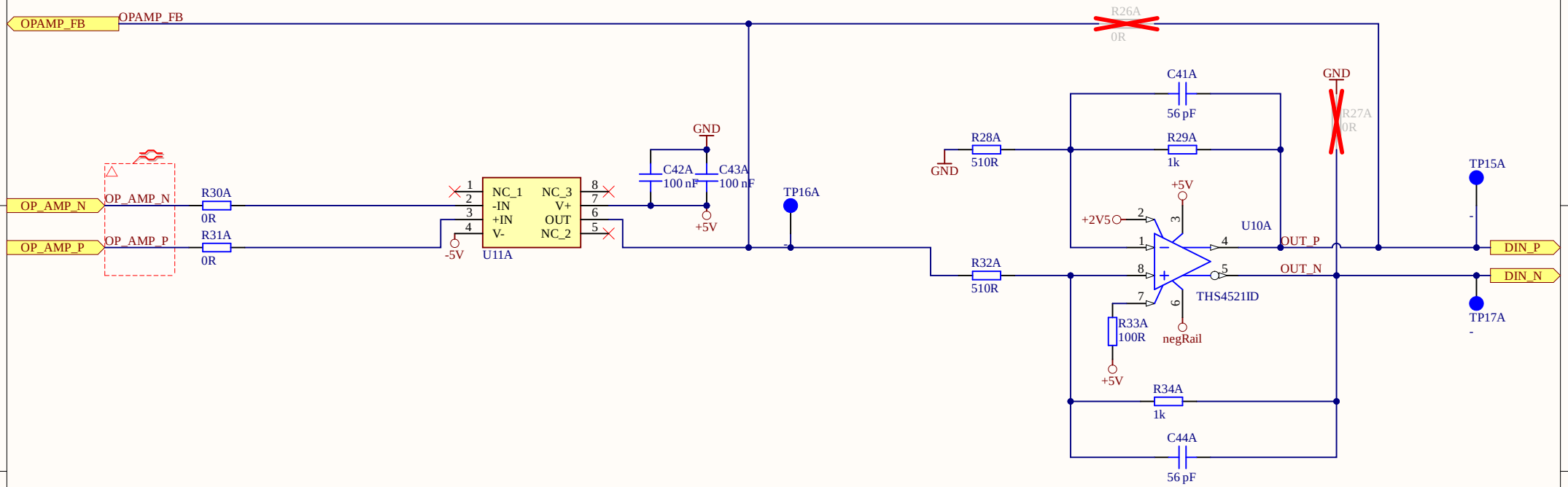
to map 5V -> 4.096V
gains needs to be 4.096V/5 = 0.8192
with R24 = 1k and R43 = 820R , resulting in a gain of g=0.82
we get a gain accuracy of 0.1%
this would allow to use 0V and 5V as rails
with Vcom = 2.5V

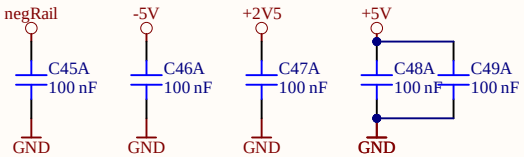
https://jansson.us/resistors.html

10 Power Supply Recommendations

The THS452x family is principally intended to operate with a nominal single-supply voltage of +3 V to +5 V. Supply-voltage tolerances are supported with the specified operating range of 2.5 V (10% low on a 3-V nominal supply) and 5.5 V (8% high on a 5-V nominal supply). Supply decoupling is required, as described in the *Application and Implementation*. Split (or bipolar) supplies can be used with the THS452x family, as long as the total value across the device remains less than 5.5 V (absolute maximum).

Using a negative supply to deliver a true swing to ground output in driving SAR ADCs may be desired. While the THS452x family quotes a rail-to-rail output, linear operation requires approximately a 200-mV headroom to the supply rails. One easy option for extending the linear output swing to ground is to provide the small negative supply voltage required using the LM7705 fixed –230-mV, negative-supply generator. This low-cost, fixed negative-supply generator accepts the 3- to 5-V positive supply input used by the THS452x and provides a –230-mV supply for the negative rail. Using the LM7705 provides an effective solution, as shown in the TI Designs TIDU187, Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts.





NC denotes no internal connection

kleine negative Spannung um das negative Rail des differentiellen OpAmps THS4521 zu versorgen, s. Kapitel 11 Datenblatt THS4561. --> rail-to-rail

Power down. PD = logic low puts device into low-power mode. PD = logic high or open for normal operation

Title OpAmp_Channnels.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 9.1 of 24

OP & Differential AMPs 1-8

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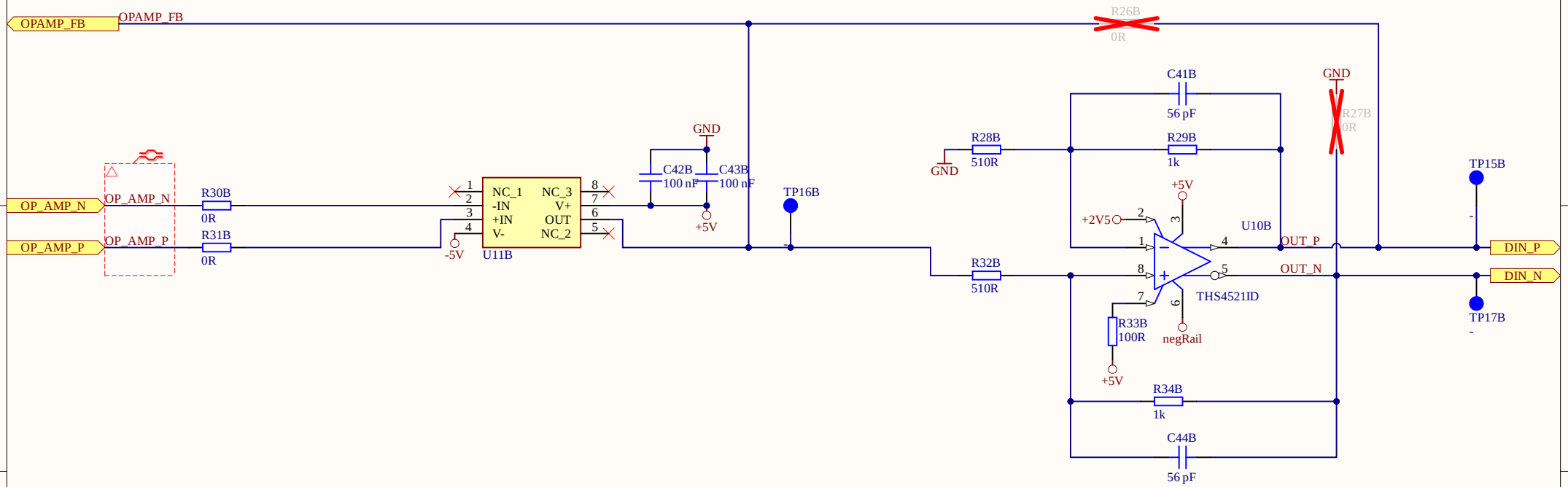

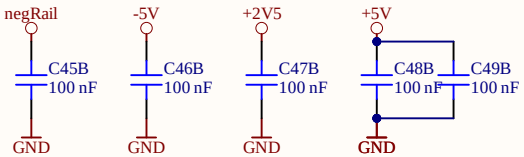

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Title OpAmp_Channnels.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 9.2 of 24

OP & Differential AMPs 1-8

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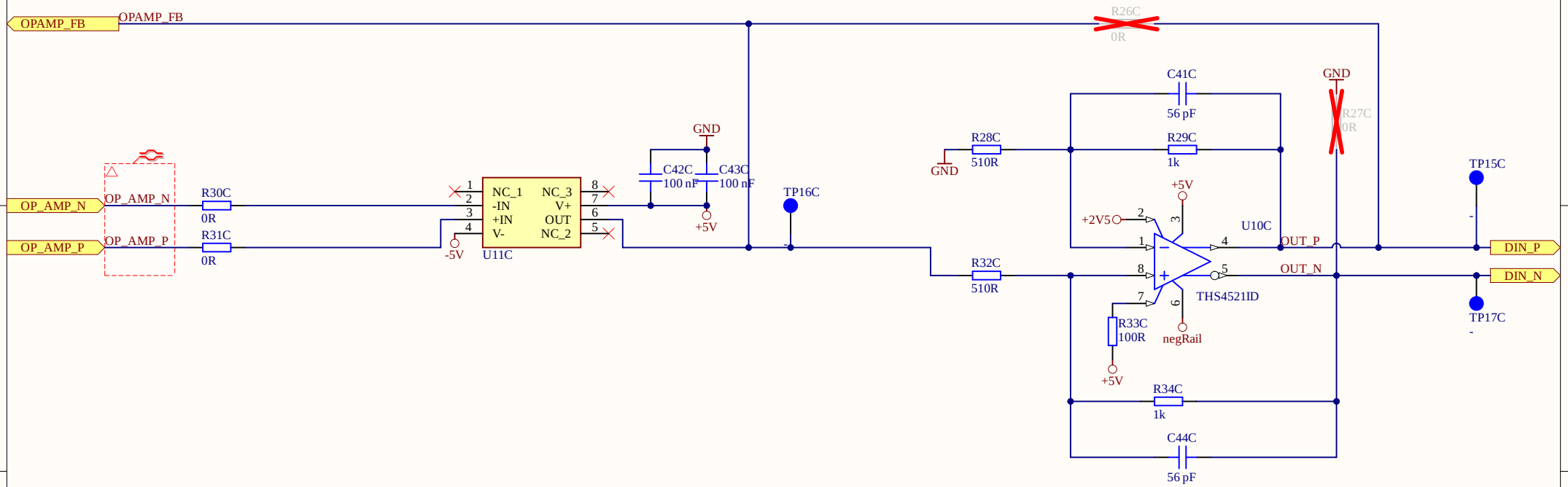

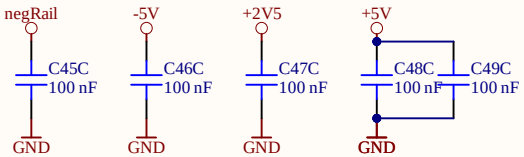

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Title OpAmp_Channnels.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 9.3 of 24

OP & Differential AMPs 1-8

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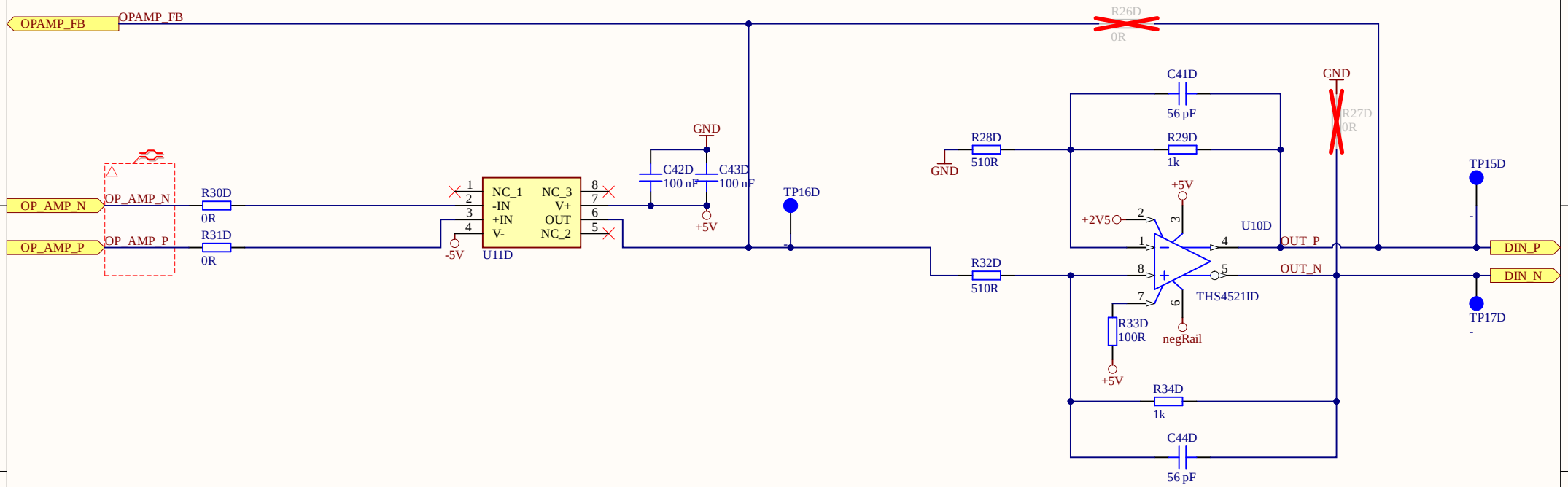

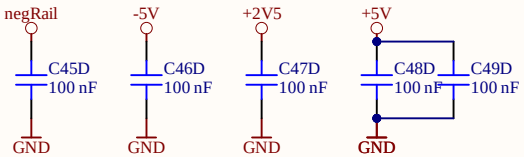

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Title OpAmp_Channnels.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 9.4 of 24

OP & Differential AMPs 1-8

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10 Power Supply Recommendations

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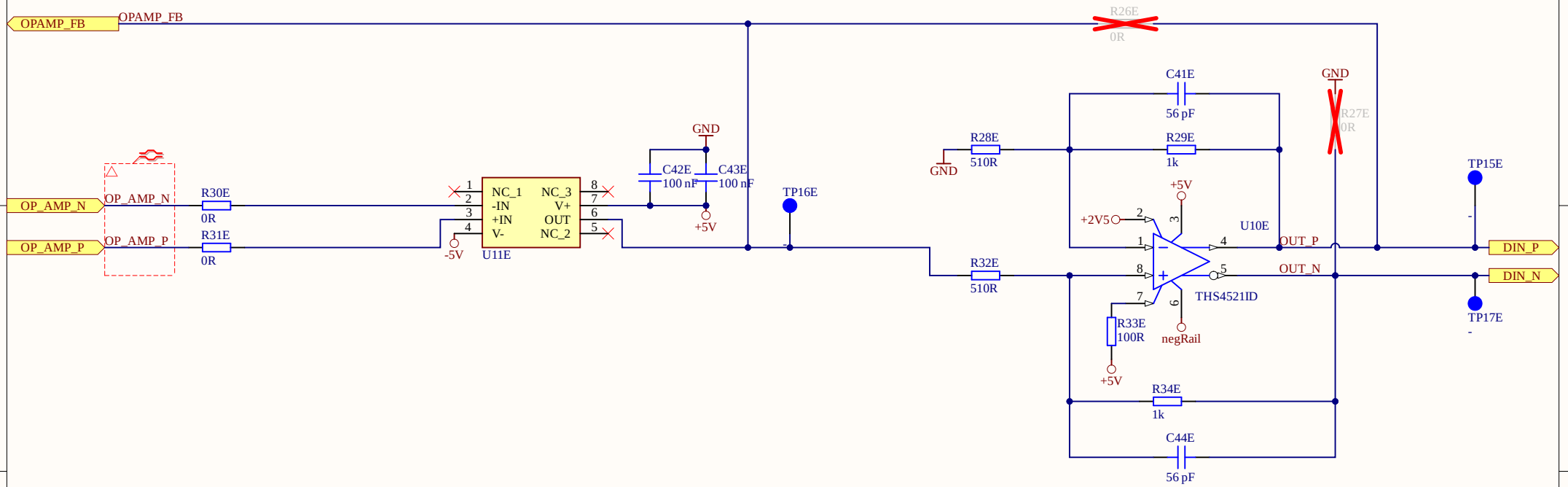

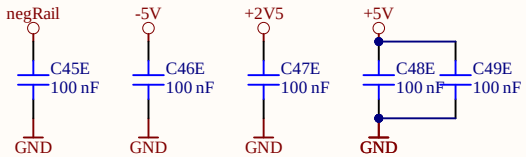

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Title OpAmp_Channnels.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 9.5 of 24

OP & Differential AMPs 1-8

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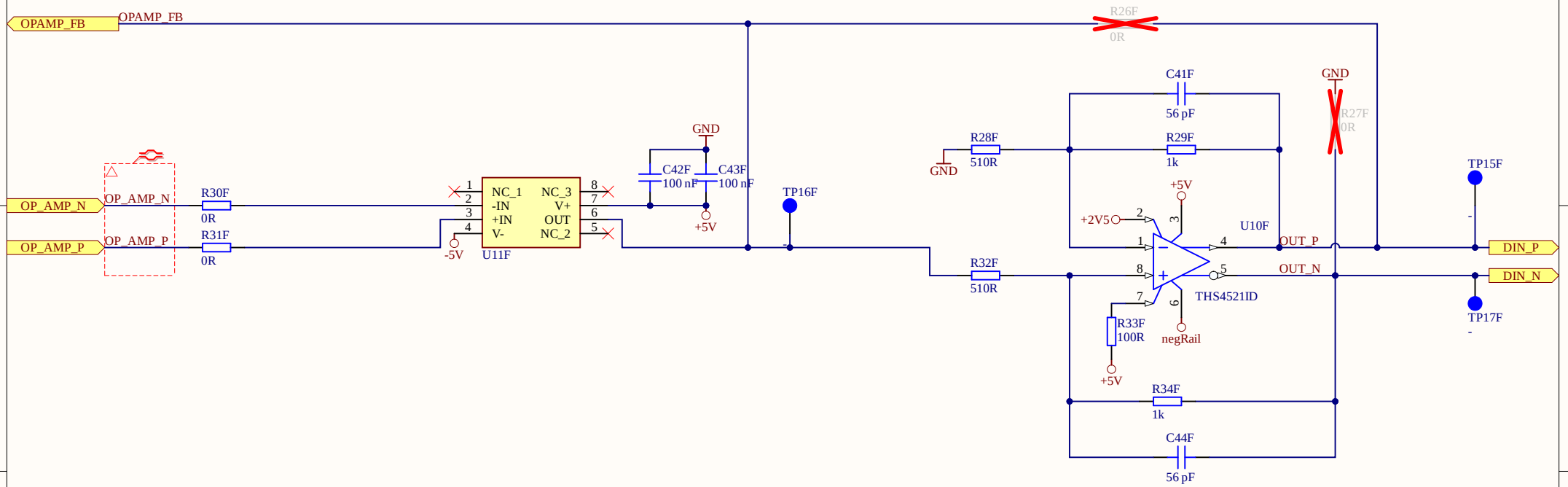

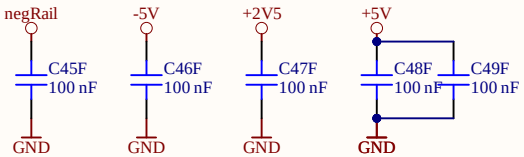

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Title OpAmp_Channnels.SchDoc		*
Revision: Rev01	Design Engineer: M. Hlatky	
Project: UZ_A_DAC.PrjPcb		Date: 09.05.2022
		Sheet 9.6 of 24

OP & Differential AMPs 1-8

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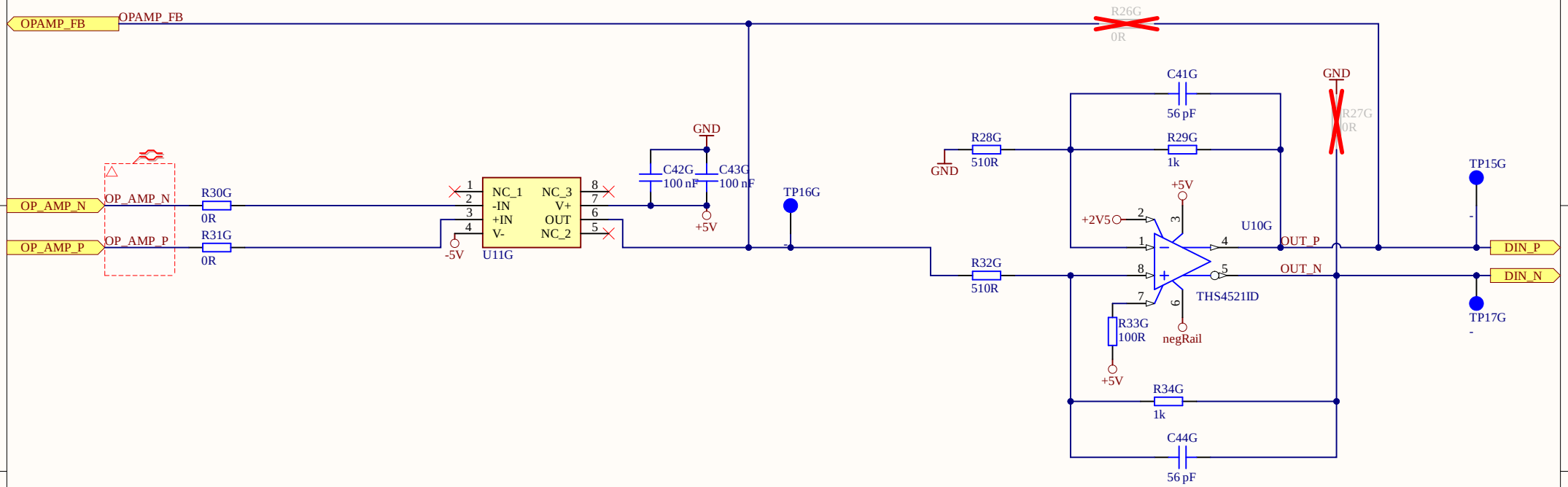
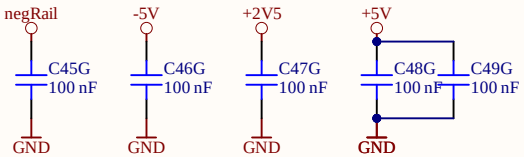
Using a negative supply to deliver a true swing to ground output in driving SAR ADCs may be desired. While the THS452x family quotes a rail-to-rail output, linear operation requires approximately a 200-mV headroom to the supply rails. One easy option for extending the linear output swing to ground is to provide the small negative supply voltage required using the LM7705 fixed –230-mV, negative-supply generator. This low-cost, fixed negative-supply generator accepts the 3- to 5-V positive supply input used by the THS452x and provides a –230-mV supply for the negative rail. Using the LM7705 provides an effective solution, as shown in the TI Designs TIDU187, Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts.





NC denotes no internal connection

kleine negative Spannung um das negative Rail des differentiellen OpAmps THS4521 zu versorgen, s. Kapitel 11 Datenblatt THS4561 --> rail-to-rail

Power down. PD = logic low puts device into low-power mode. PD = logic high or open for normal operation

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OP & Differential AMPs 1-8

to map 5V -> 4.096V
gains needs to be 4.096V/5 = 0.8192
with R24 = 1k and R43 = 820R , resulting in a gain of g=0.82
we get a gain accuracy of 0.1%
this would allow to use 0V and 5V as rails
with Vcom = 2.5V

https://jansson.us/resistors.html

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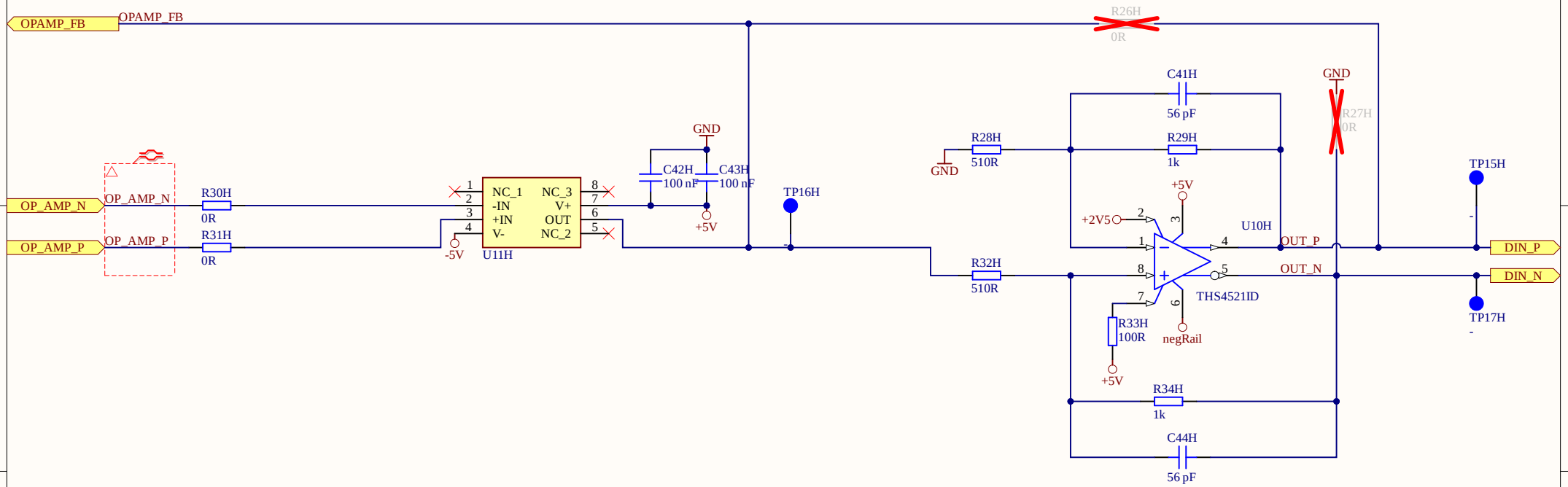

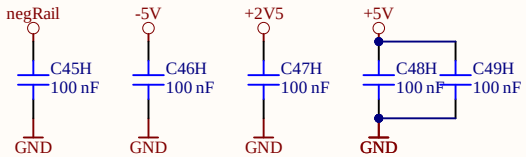

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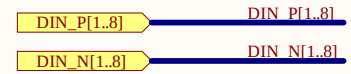
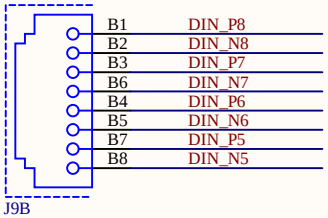
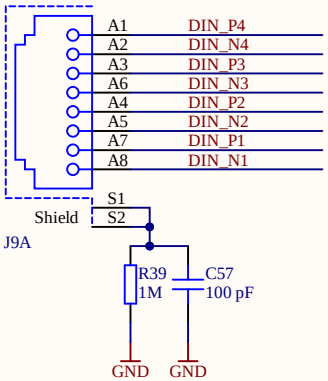
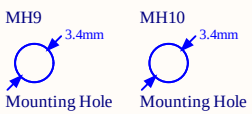
Ethernet Connector for HITL

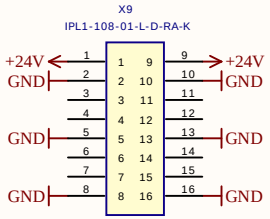
When using the VIN (24V) on the power connector X1, use pin 2 and 10 as return ground

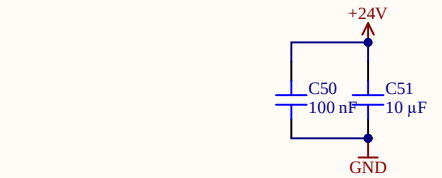


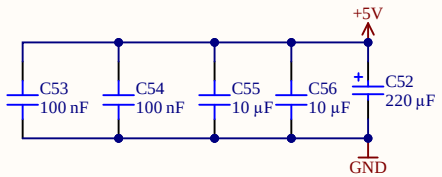


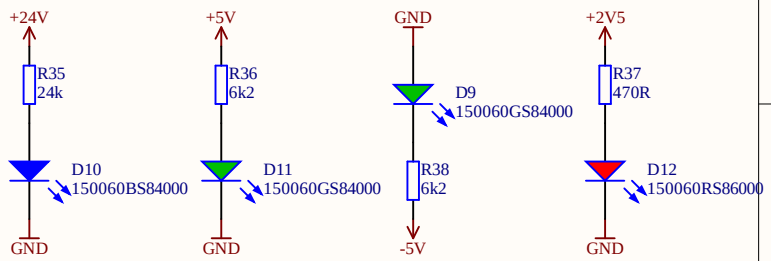












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