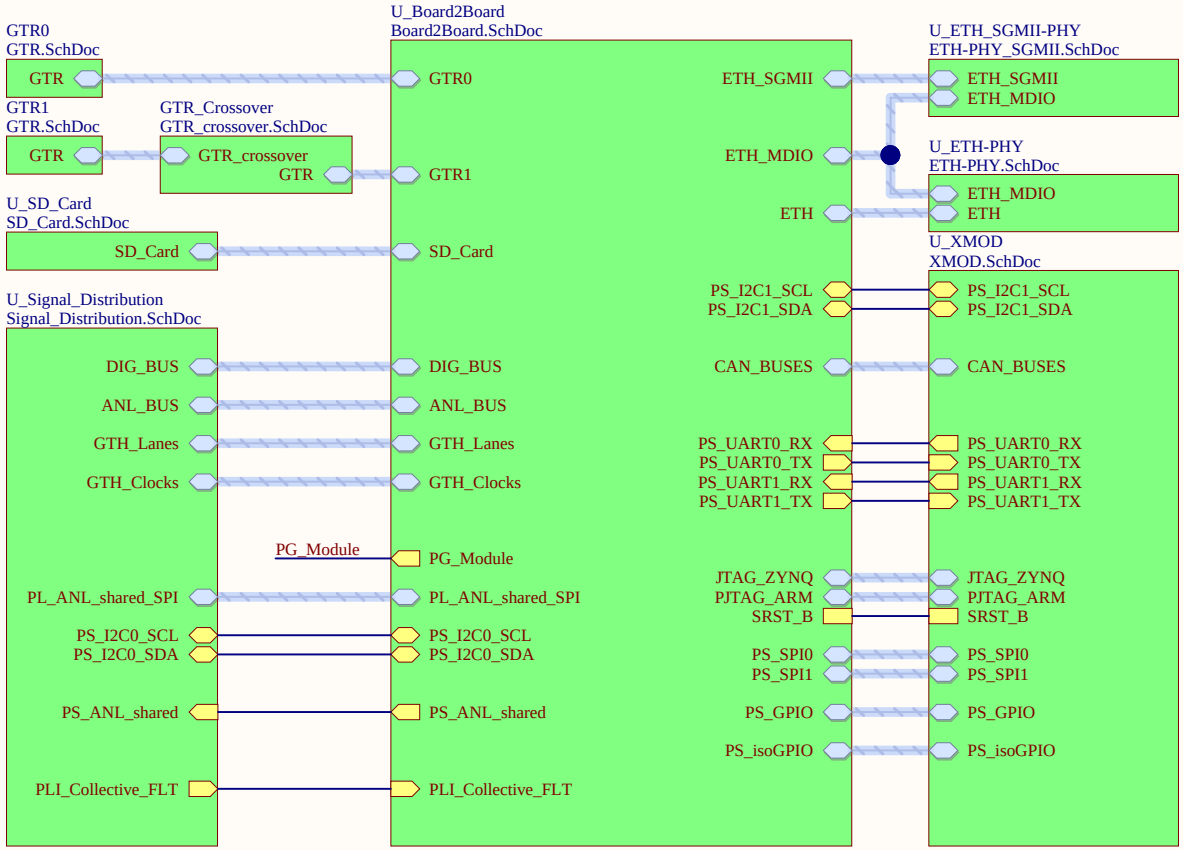
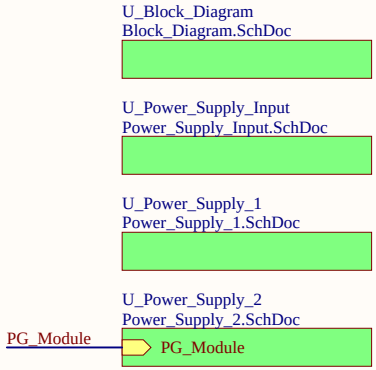
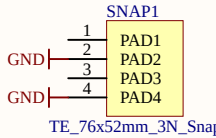
UltraZohm Carrier Board

For more information visit: www.ultrazohm.com

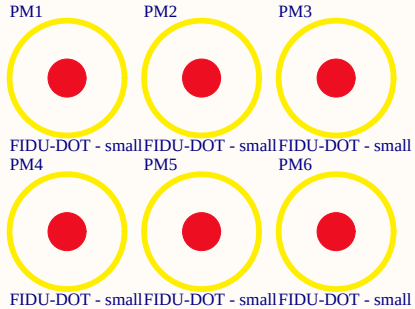




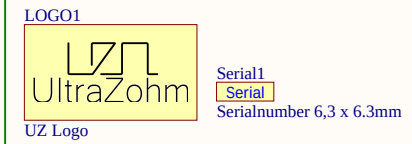
Mounting holes SoM



Fiducials

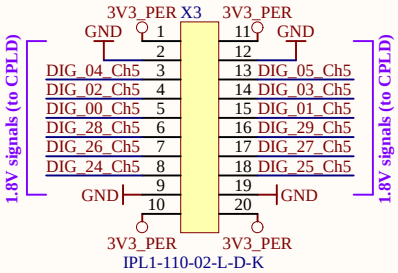


design information, revision number, ...

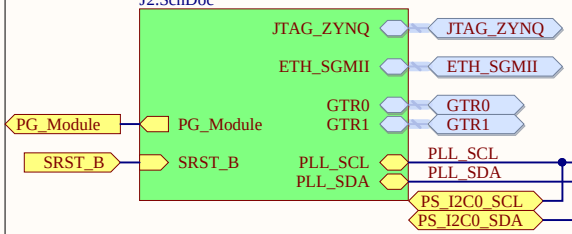


Title CarrierBoard_TopSheet.SchDoc		***UltraZohm***	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 1 of 36	

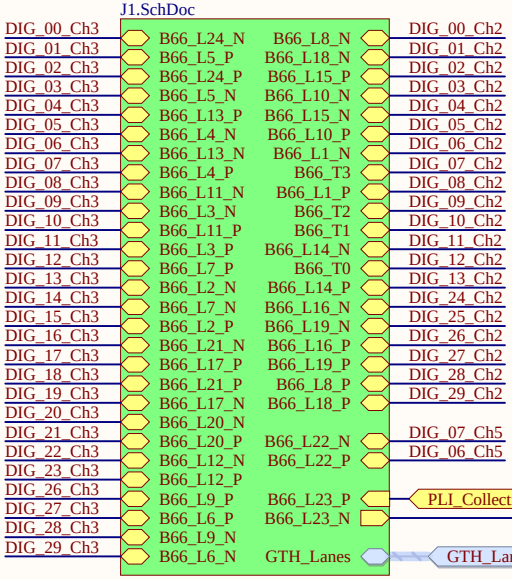
The 5th digital socket is not full connected with FPGA pins. DIG_00...DIG05 and DIG_24...DIG_29 of this socket can be used externally via this connector.



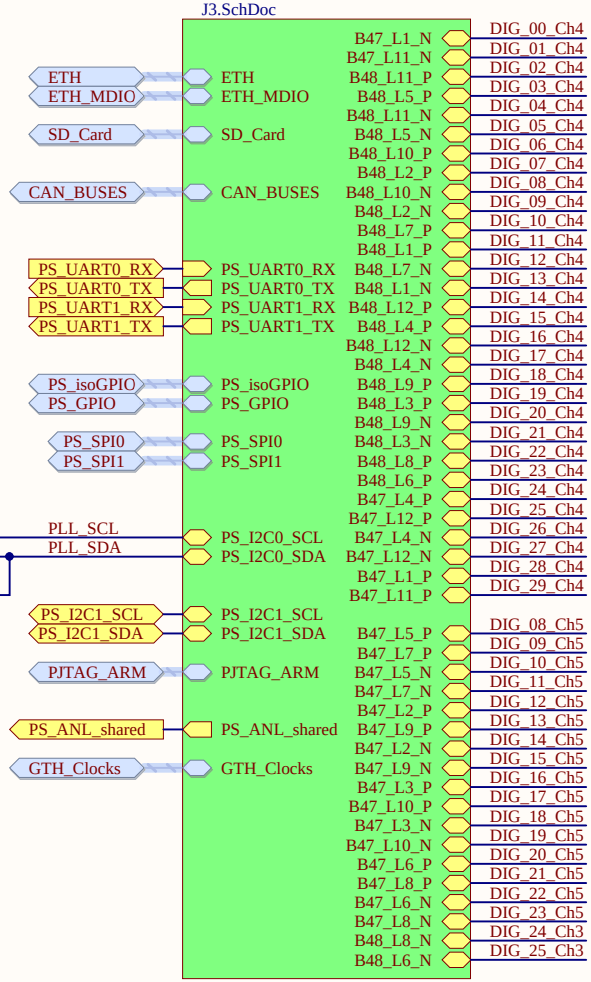
U_J2
J2.SchDoc



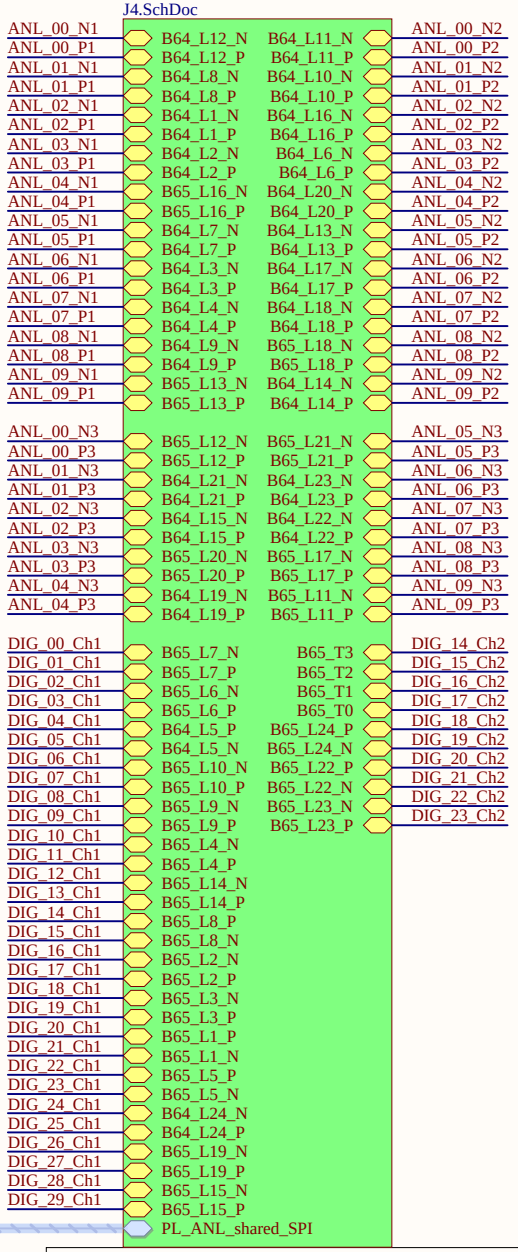
U_J1
J1.SchDoc



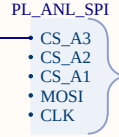
U_J3
J3.SchDoc



U_J4
J4.SchDoc

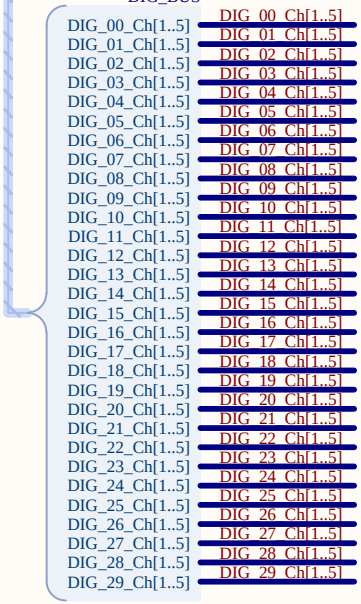


PL_ANL_SPI

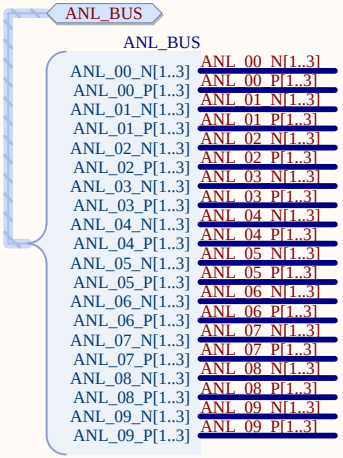


The other signals are assigned in J4

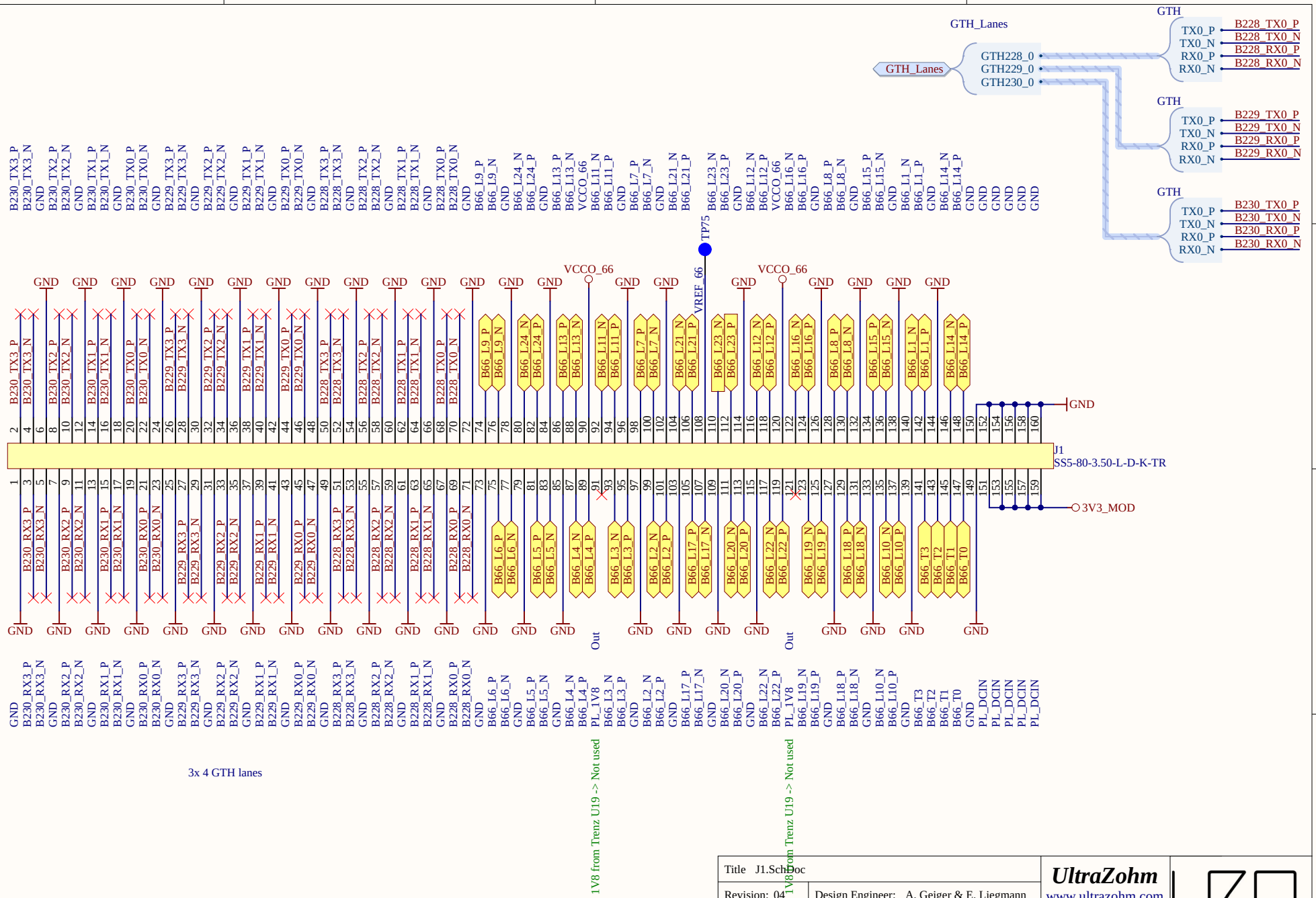
DIG_BUS



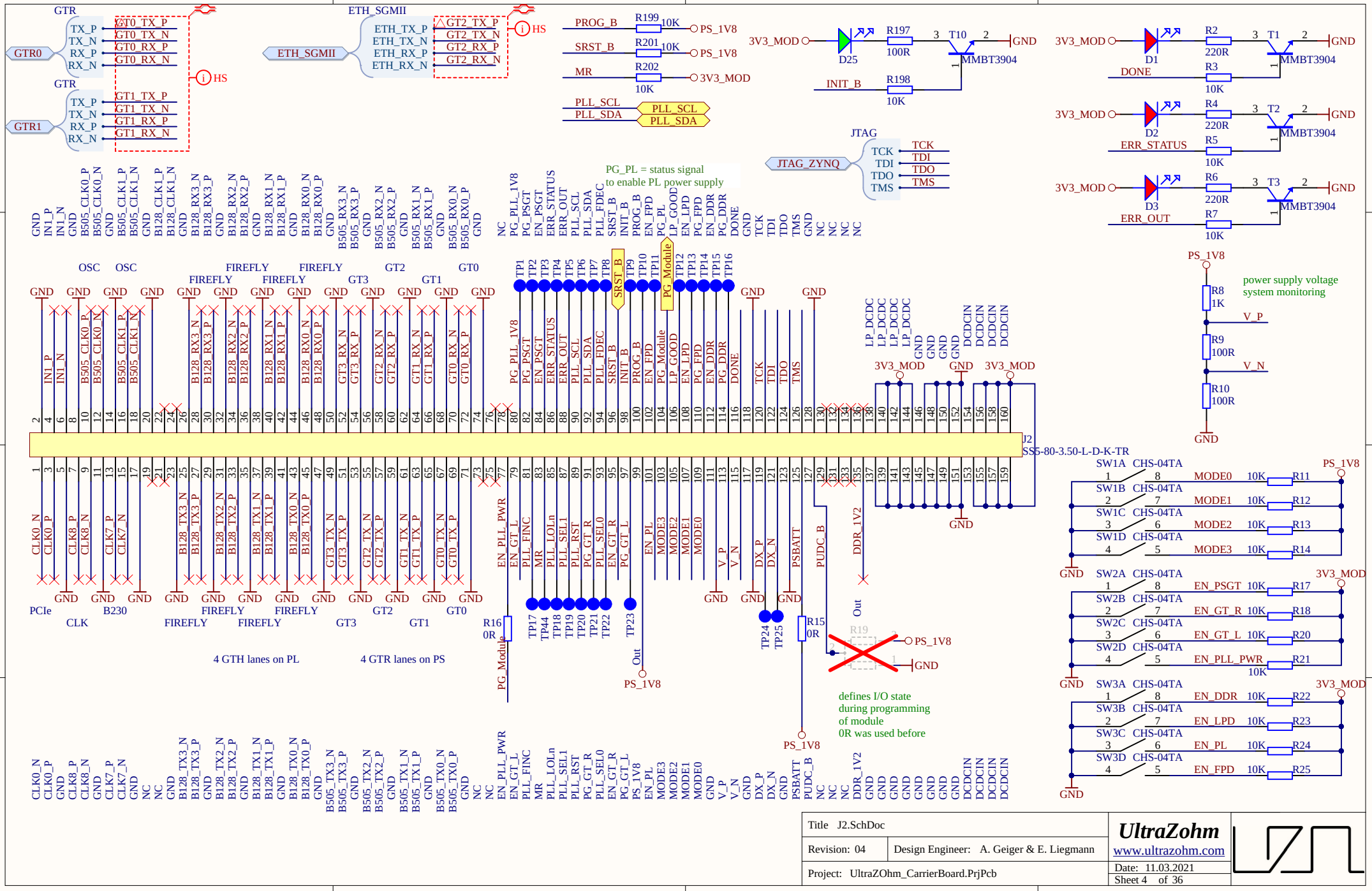
ANL_BUS



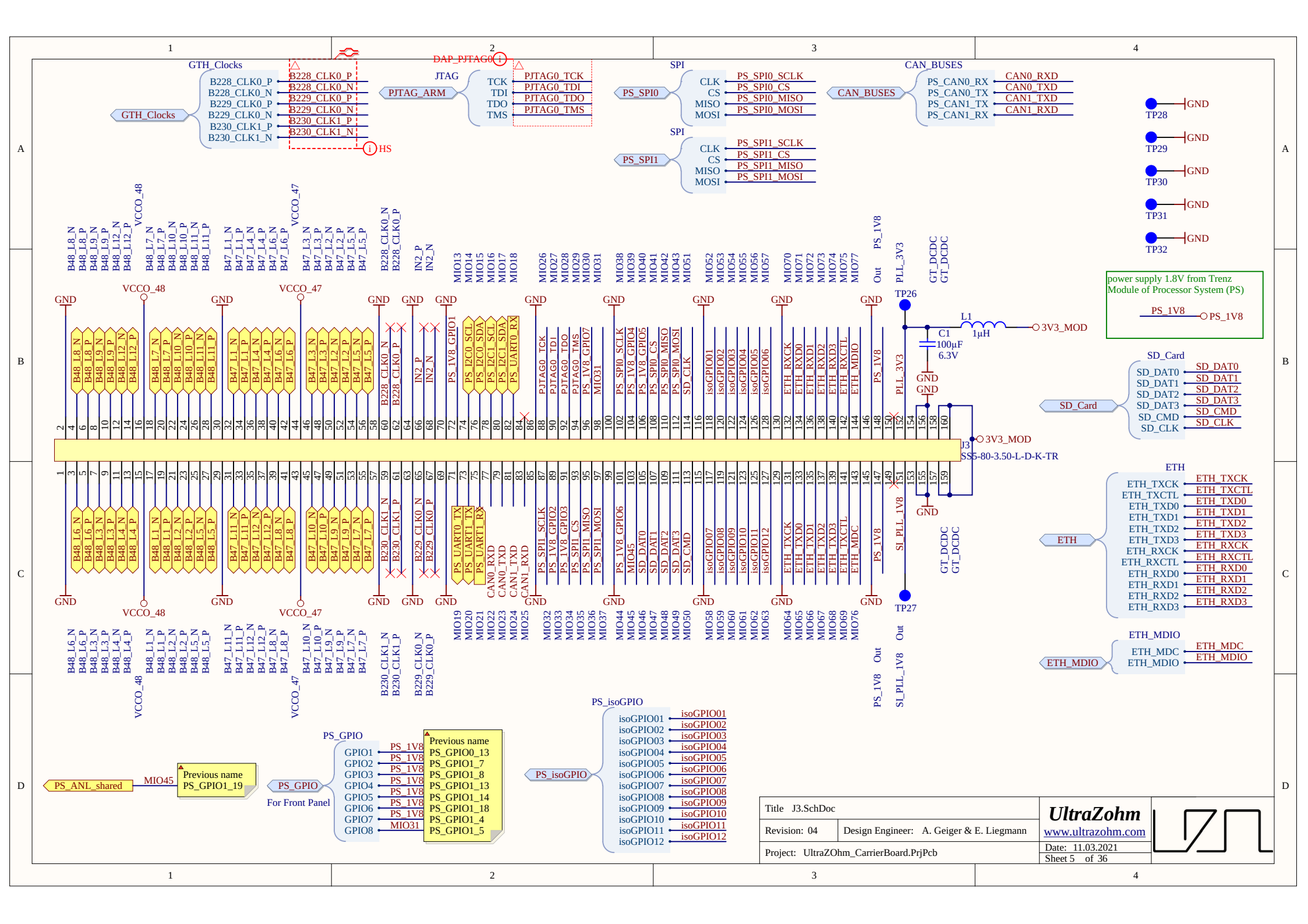
Title Board2Board.SchDoc		UltraZohm www.ultrazohm.com
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 2 of 36



Title J1.SchDoc		UltraZohm www.ultrazohm.com
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	Date: 11.03.2021
Project: UltraZOhm_CarrierBoard.PrjPcb		Sheet 3 of 36



Title J2.SchDoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 4 of 36	


GTH_Clocks
B228_CLK0_P
B228_CLK0_N
B229_CLK0_P
B229_CLK0_N
B230_CLK1_P
B230_CLK1_N
HS
DAP_PJTAG0
JTAG
PJTAG_ARM
TCK
TDI
TDO
TMS
PJTAG0_TCK
PJTAG0_TDI
PJTAG0_TDO
PJTAG0_TMS
SPI
PS_SPI0
CLK
CS
MISO
MOSI
PS_SPI0_SCLK
PS_SPI0_CS
PS_SPI0_MISO
PS_SPI0_MOSI
PS_SPI1
PS_SPI1_SCLK
PS_SPI1_CS
PS_SPI1_MISO
PS_SPI1_MOSI
CAN_BUSES
PS_CAN0_RX
PS_CAN0_TX
PS_CAN1_TX
PS_CAN1_RX
CAN0_RXD
CAN0_TXD
CAN1_TXD
CAN1_RXD
TP28
TP29
TP30
TP31
TP32
GND
power supply 1.8V from Trenz Module of Processor System (PS)
PS_1V8
TP26
TP27
L1
1µH
C1
100µF
6.3V
3V3_MOD
J3
SS5-80-3.50-L-D-K-TR
SD_Card
SD_DAT0
SD_DAT1
SD_DAT2
SD_DAT3
SD_CMD
SD_CLK
ETH
ETH_TXCK
ETH_TXCTL
ETH_TXD0
ETH_TXD1
ETH_TXD2
ETH_TXD3
ETH_RXCK
ETH_RXCTL
ETH_RXD0
ETH_RXD1
ETH_RXD2
ETH_RXD3
ETH_MDIO
ETH_MDC
PS_ANL_shared
MIO45
Previous name
PS_GPIO1_19
PS_GPIO
For Front Panel
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
Previous name
PS_GPIO0_13
PS_GPIO1_7
PS_GPIO1_8
PS_GPIO1_13
PS_GPIO1_14
PS_GPIO1_18
PS_GPIO1_4
PS_GPIO1_5
PS_isoGPIO
isoGPIO01
isoGPIO02
isoGPIO03
isoGPIO04
isoGPIO05
isoGPIO06
isoGPIO07
isoGPIO08
isoGPIO09
isoGPIO10
isoGPIO11
isoGPIO12
Title J3.SchDoc
Revision: 04
Design Engineer: A. Geiger & E. Liegmann
Project: UltraZOhm_CarrierBoard.PrjPcb
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Date: 11.03.2021
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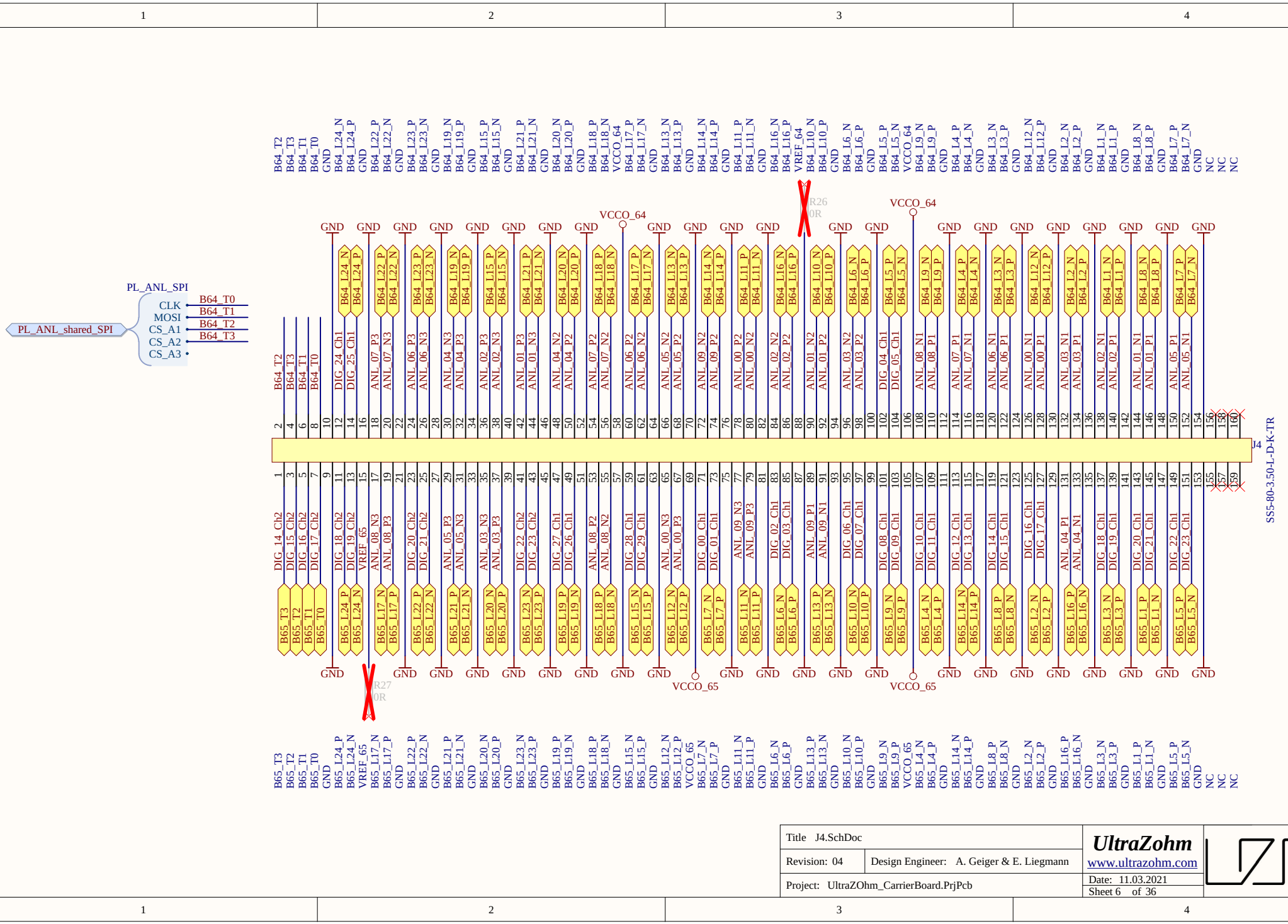
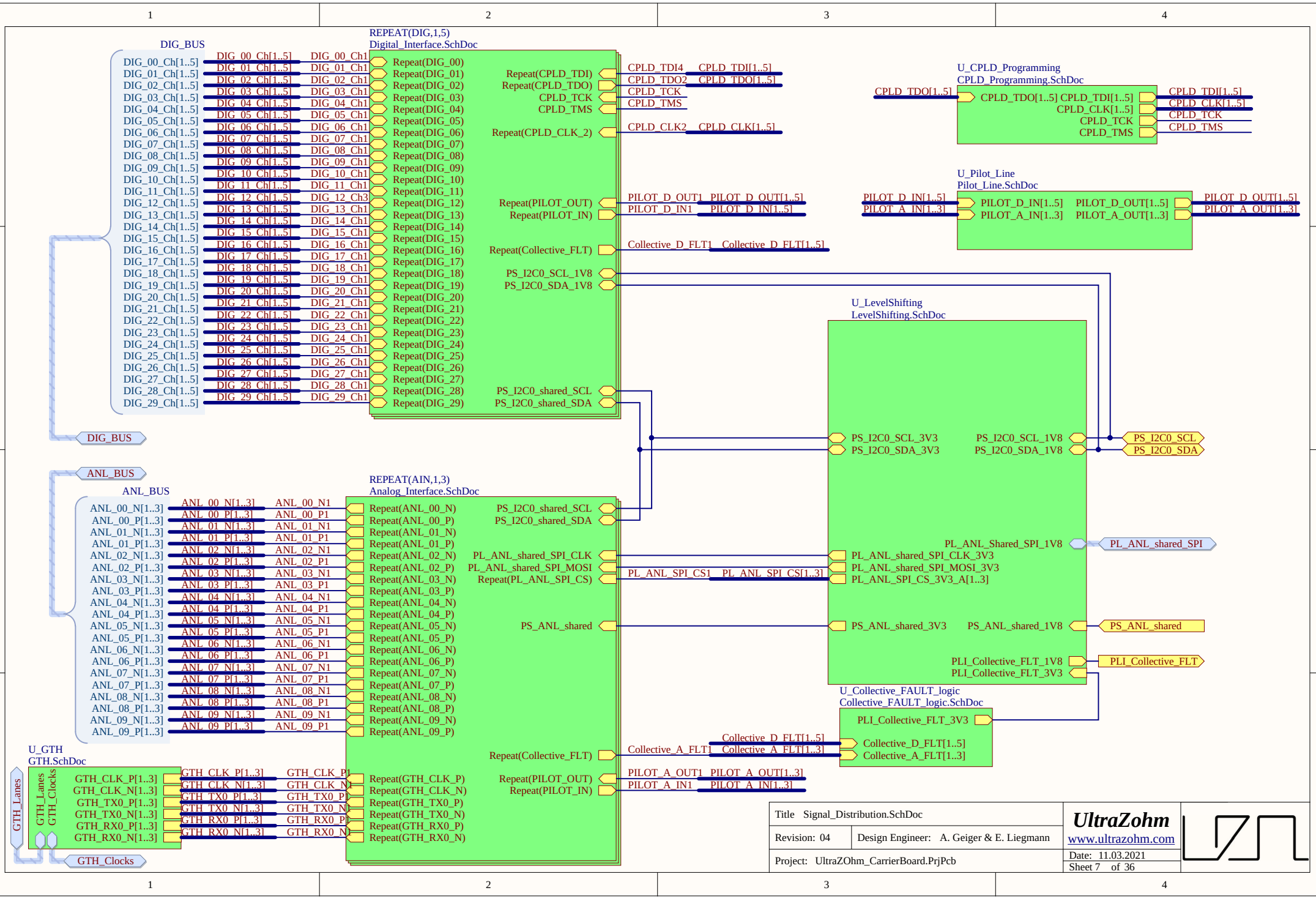


Title J4.SchDoc		UltraZohm www.ultrazohm.com
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 6 of 36


DIG_BUS
REPEAT(DIG,1,5)
Digital_Interface.SchDoc
Repeat(CPLD_TDI)
Repeat(CPLD_TDO)
CPLD_TCK
CPLD_TMS
Repeat(CPLD_CLK_2)
Repeat(PILOT_OUT)
Repeat(PILOT_IN)
Repeat(Collective_FLT)
PS_I2C0_SCL_1V8
PS_I2C0_SDA_1V8
PS_I2C0_shared_SCL
PS_I2C0_shared_SDA
CPLD_TDI4
CPLD_TDO2
CPLD_TDI[1..5]
CPLD_TDO[1..5]
CPLD_CLK2
CPLD_CLK[1..5]
PILOT_D_OUT1
PILOT_D_OUT[1..5]
PILOT_D_IN1
PILOT_D_IN[1..5]
Collective_D_FLT1
Collective_D_FLT[1..5]
U_CPLD_Programming
CPLD_Programming.SchDoc
CPLD_TDO[1..5]
CPLD_TDI[1..5]
CPLD_CLK[1..5]
CPLD_TCK
CPLD_TMS
U_Pilot_Line
Pilot_Line.SchDoc
PILOT_D_IN[1..5]
PILOT_A_IN[1..3]
PILOT_D_OUT[1..5]
PILOT_A_OUT[1..3]
U_LevelShifting
LevelShifting.SchDoc
PS_I2C0_SCL_3V3
PS_I2C0_SDA_3V3
PS_I2C0_SCL_1V8
PS_I2C0_SDA_1V8
PS_I2C0_SCL
PS_I2C0_SDA
PL_ANL_Shared_SPI_1V8
PL_ANL_shared_SPI
PL_ANL_shared_SPI_CLK_3V3
PL_ANL_shared_SPI_MOSI_3V3
PL_ANL_SPI_CS_3V3_A[1..3]
PS_ANL_shared_3V3
PS_ANL_shared_1V8
PS_ANL_shared
PLI_Collective_FLT_1V8
PLI_Collective_FLT_3V3
PLI_Collective_FLT
U_Collective_FAULT_logic
Collective_FAULT_logic.SchDoc
PLI_Collective_FLT_3V3
Collective_D_FLT[1..5]
Collective_A_FLT[1..3]
ANL_BUS
REPEAT(AIN,1,3)
Analog_Interface.SchDoc
PS_I2C0_shared_SCL
PS_I2C0_shared_SDA
PL_ANL_shared_SPI_CLK
PL_ANL_shared_SPI_MOSI
Repeat(PL_ANL_SPI_CS)
PS_ANL_shared
Repeat(Collective_FLT)
PL_ANL_SPI_CS1
PL_ANL_SPI_CS[1..3]
Collective_A_FLT1
Collective_A_FLT[1..3]
U_GTH
GTH.SchDoc
GTH_Lanes
GTH_Clocks
GTH_CLK_P[1..3]
GTH_CLK_N[1..3]
GTH_TX0_P[1..3]
GTH_TX0_N[1..3]
GTH_RX0_P[1..3]
GTH_RX0_N[1..3]
Repeat(GTH_CLK_P)
Repeat(GTH_CLK_N)
Repeat(GTH_TX0_P)
Repeat(GTH_TX0_N)
Repeat(GTH_RX0_P)
Repeat(GTH_RX0_N)
Repeat(PILOT_OUT)
Repeat(PILOT_IN)
PILOT_A_OUT1
PILOT_A_OUT[1..3]
PILOT_A_IN1
PILOT_A_IN[1..3]
Title Signal_Distribution.SchDoc
Revision: 04
Design Engineer: A. Geiger & E. Liegmann
Project: UltraZOhm_CarrierBoard.PrjPcb
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Date: 11.03.2021
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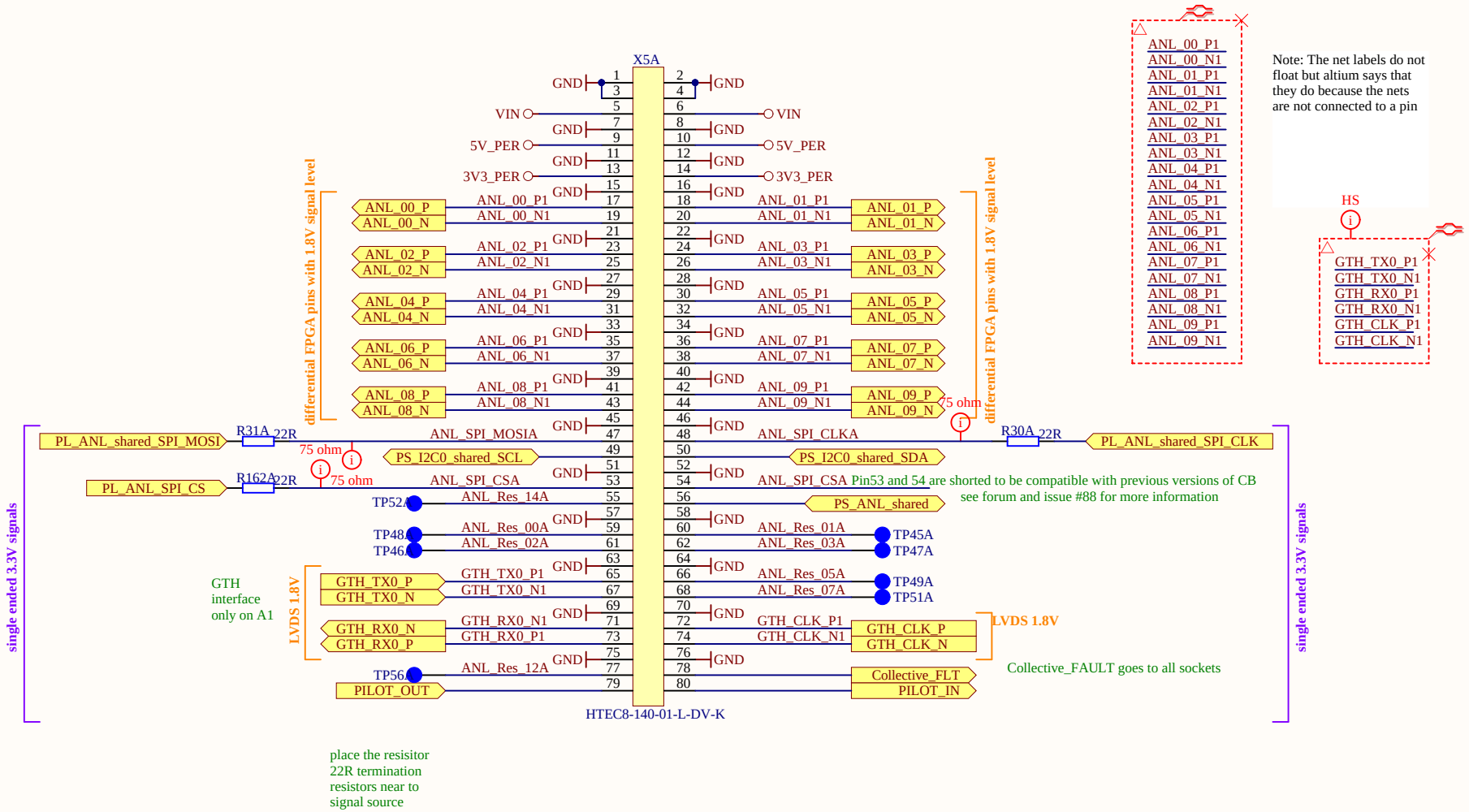
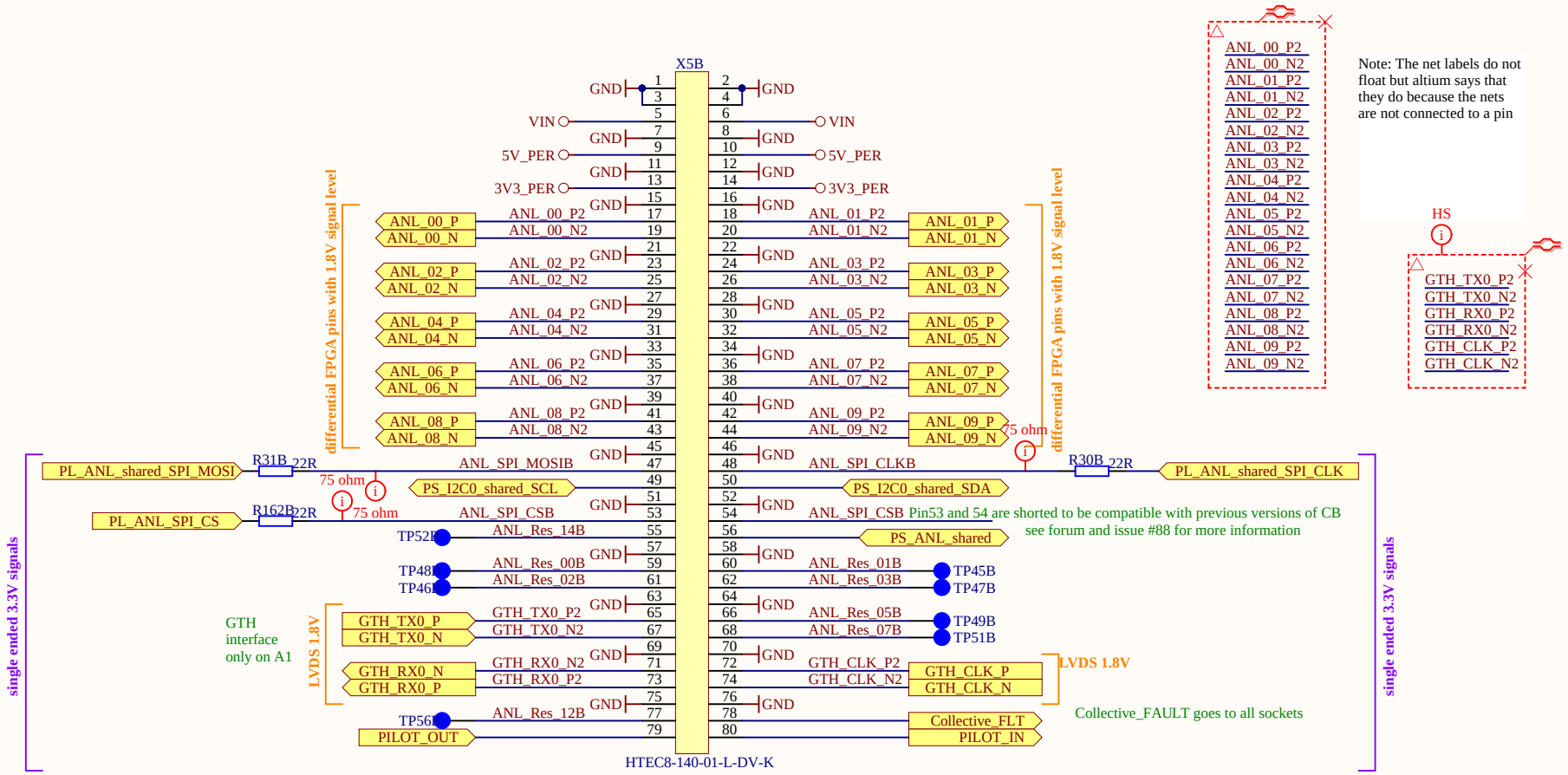
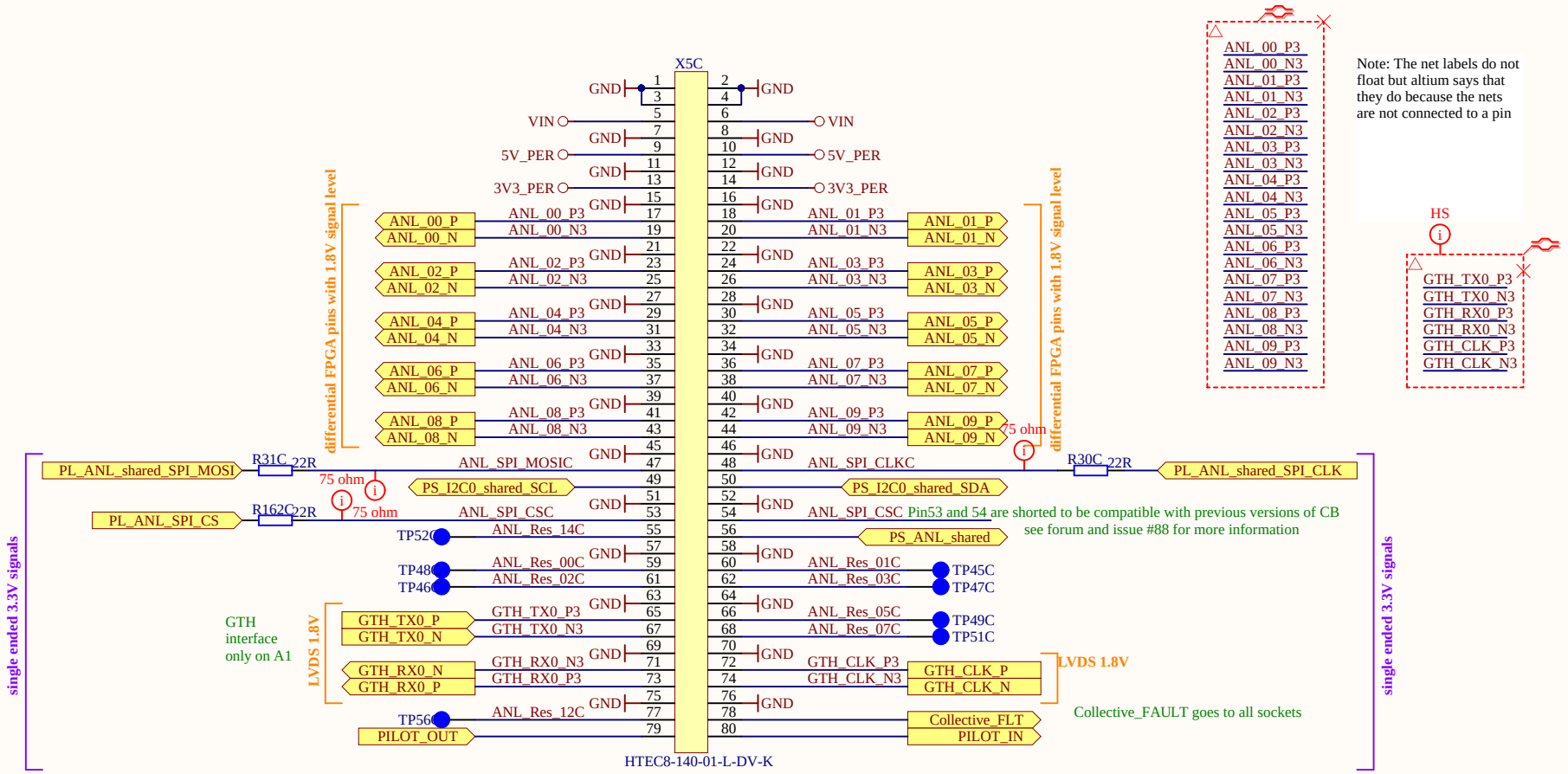


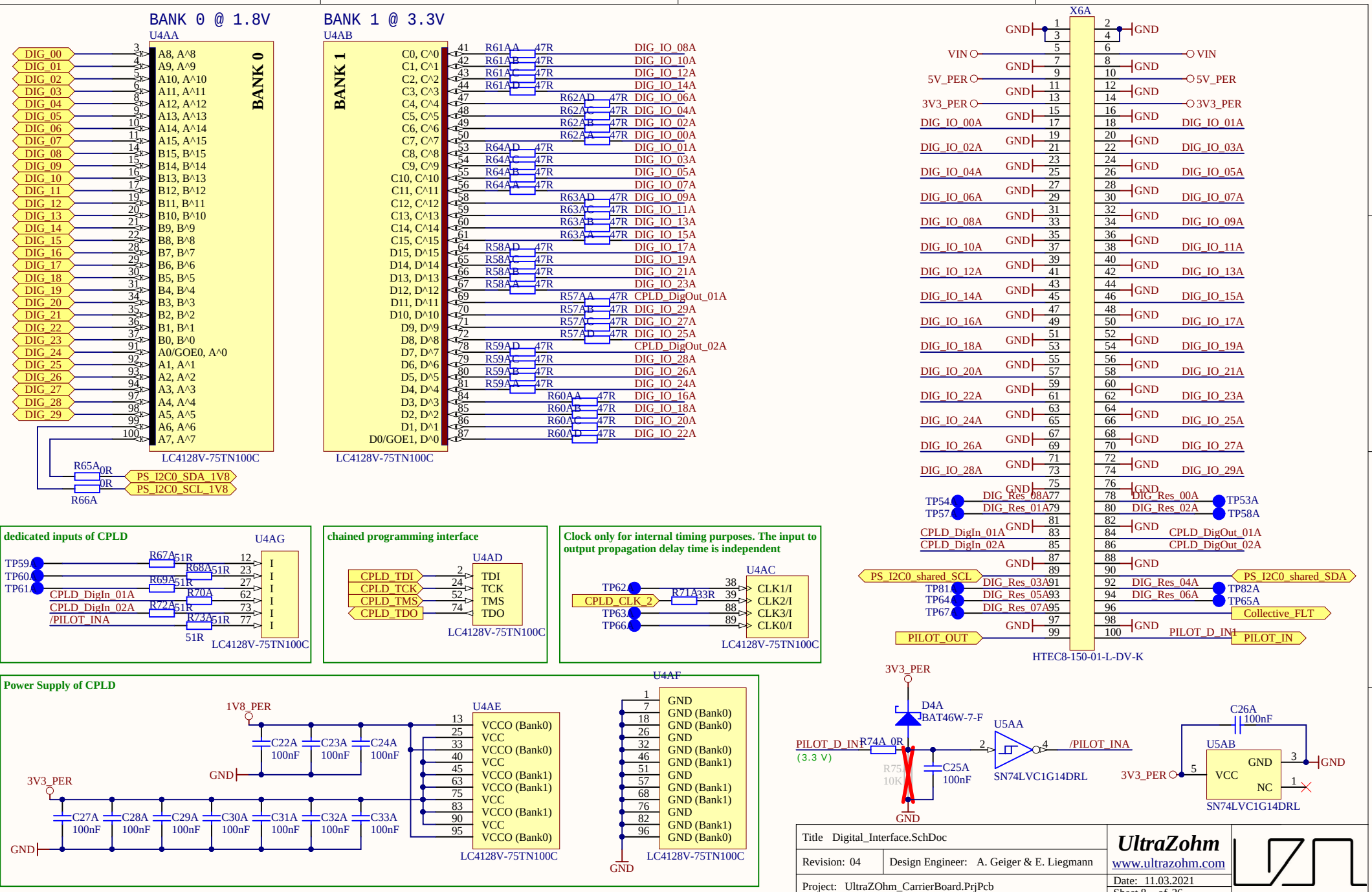
Title Analog_Interface.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	Sheet 9 of 36



Title Analog_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 9 of 36



Title Analog_Interface.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 9 of 36	



Title	Digital_Interface.SchDoc		
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	Sheet 8 of 36

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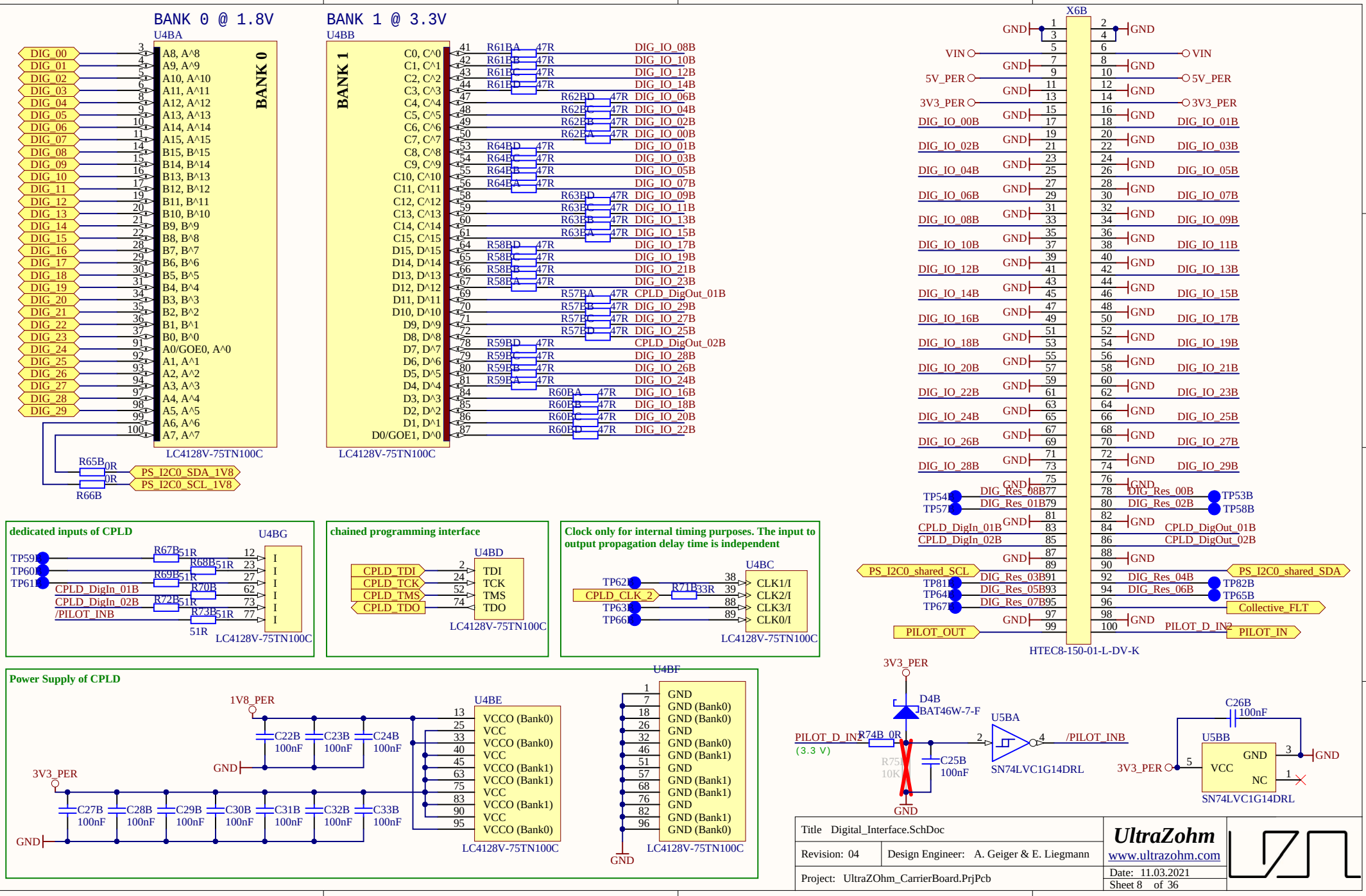
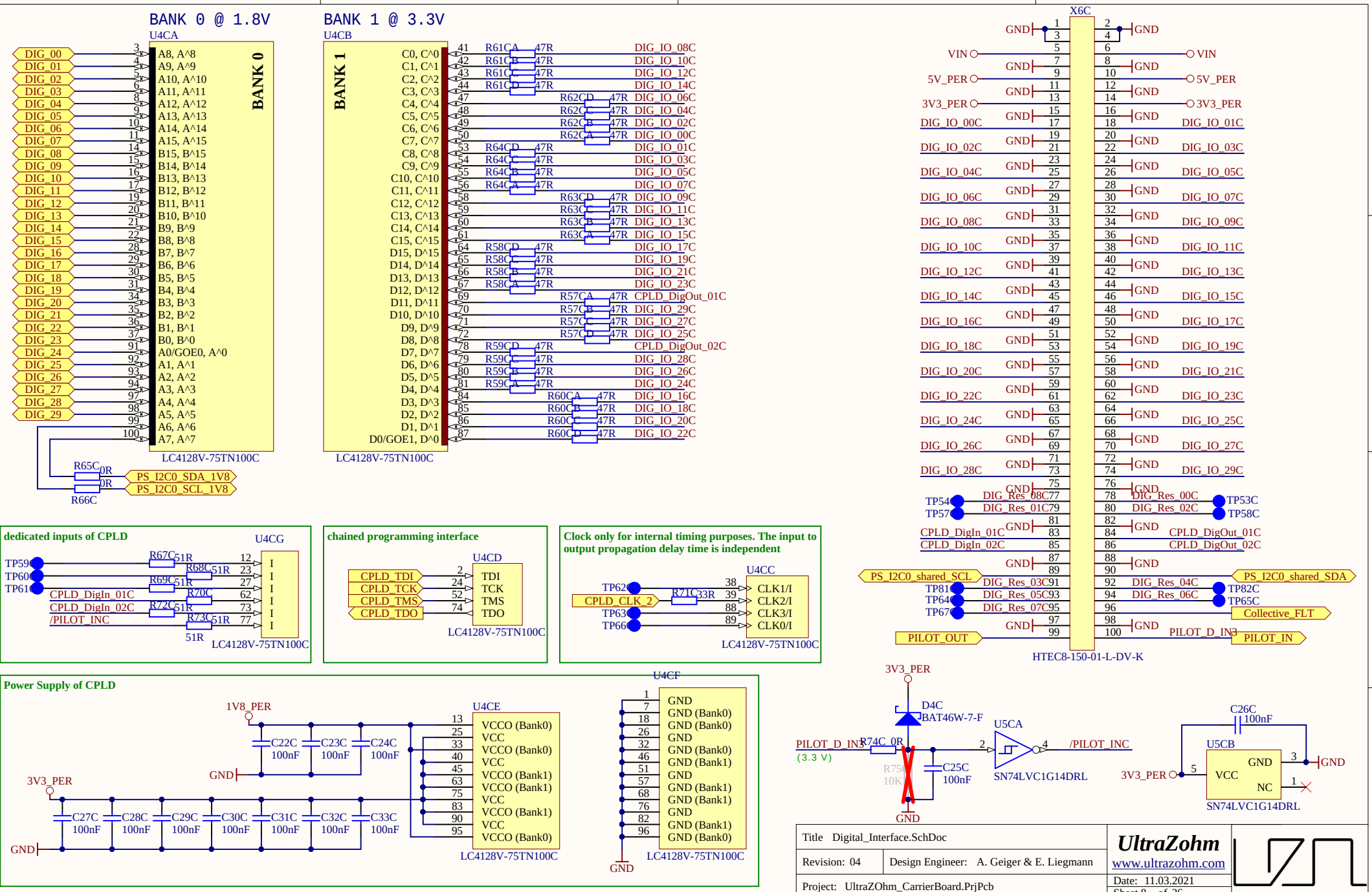
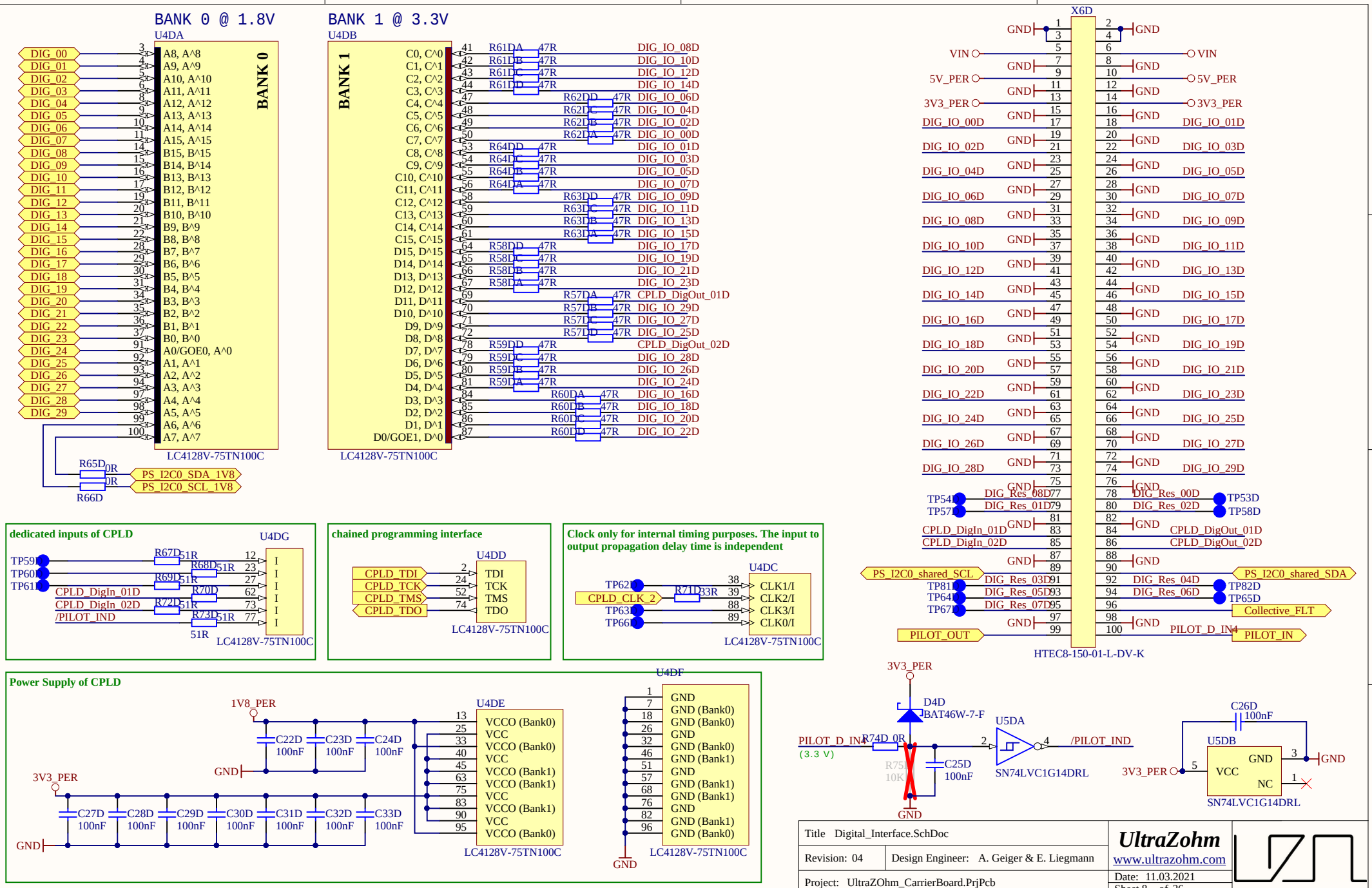
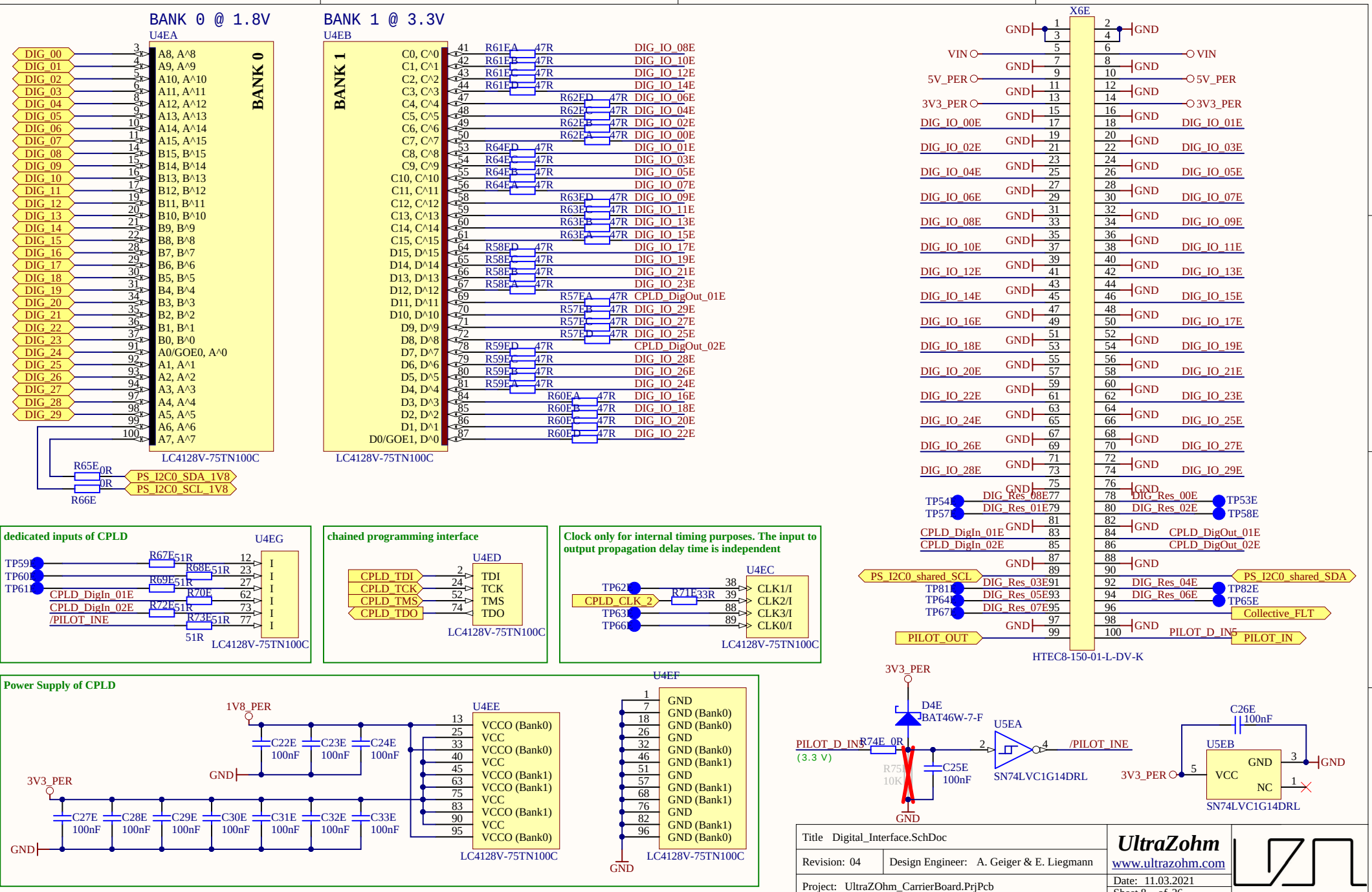
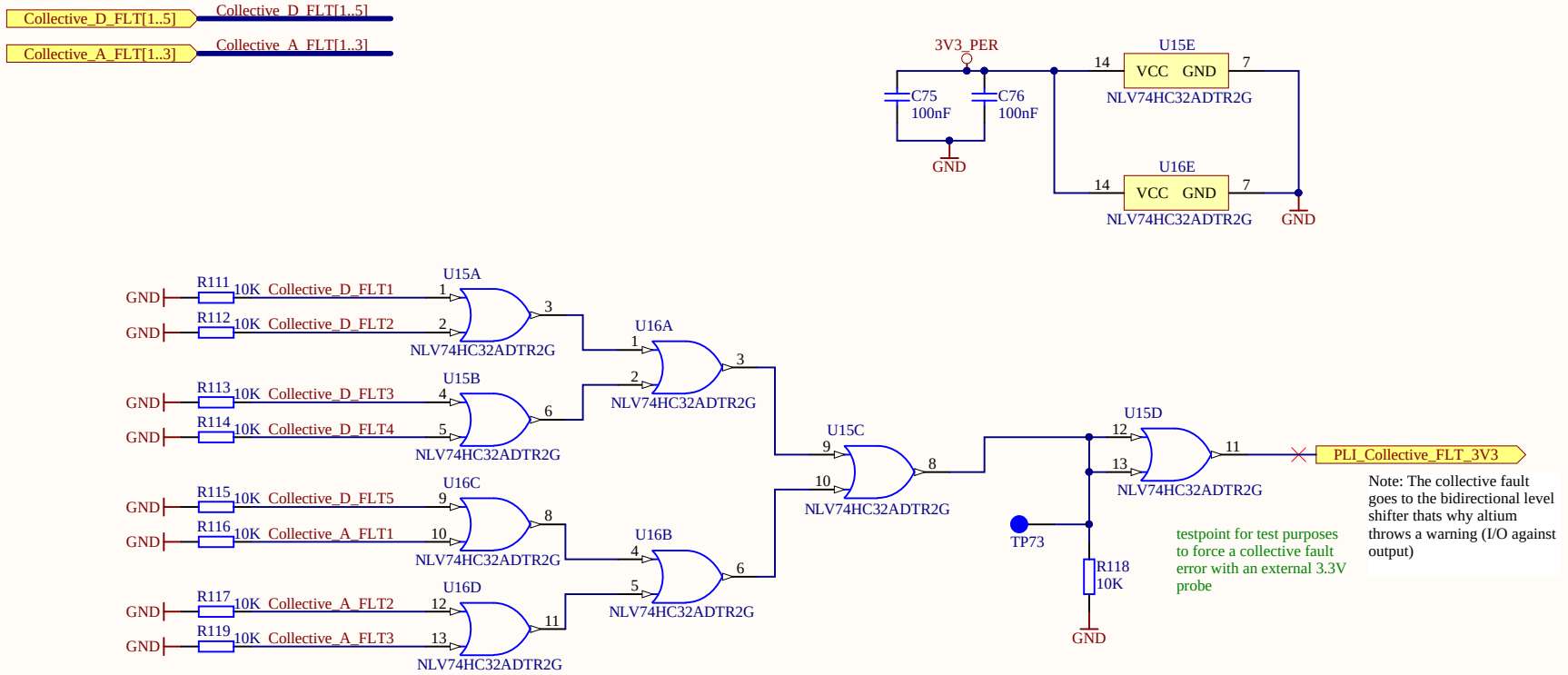

BANK 0 @ 1.8V
U4BA
BANK 0
LC4128V-75TN100C
BANK 1 @ 3.3V
U4BB
BANK 1
LC4128V-75TN100C
X6B
HTEC8-150-01-L-DV-K
dedicated inputs of CPLD
U4BG
LC4128V-75TN100C
chained programming interface
U4BD
LC4128V-75TN100C
Clock only for internal timing purposes. The input to output propagation delay time is independent
U4BC
LC4128V-75TN100C
Power Supply of CPLD
U4BE
LC4128V-75TN100C
U4BF
LC4128V-75TN100C
SN74LVC1G14DRL
SN74LVC1G14DRL
Title Digital_Interface.SchDoc
Revision: 04
Design Engineer: A. Geiger & E. Liegmann
Project: UltraZOhm_CarrierBoard.PrjPcb
UltraZohm
www.ultrazohm.com
Date: 11.03.2021
Sheet 8 of 36


BANK 0 @ 1.8V
U4CA
BANK 0
LC4128V-75TN100C
BANK 1 @ 3.3V
U4CB
BANK 1
LC4128V-75TN100C
X6C
HTEC8-150-01-L-DV-K
dedicated inputs of CPLD
U4CG
LC4128V-75TN100C
chained programming interface
U4CD
LC4128V-75TN100C
Clock only for internal timing purposes. The input to output propagation delay time is independent
U4CC
LC4128V-75TN100C
Power Supply of CPLD
U4CE
U4CF
LC4128V-75TN100C
LC4128V-75TN100C
D4C
BAT46W-7-F
U5CA
SN74LVC1G14DRL
U5CB
SN74LVC1G14DRL
Title Digital_Interface.SchDoc
Revision: 04
Design Engineer: A. Geiger & E. Liegmann
Project: UltraZOhm_CarrierBoard.PrjPcb
UltraZohm
www.ultrazohm.com
Date: 11.03.2021
Sheet 8 of 36


BANK 0 @ 1.8V
U4DA
BANK 0
A8, A^8
A9, A^9
A10, A^10
A11, A^11
A12, A^12
A13, A^13
A14, A^14
A15, A^15
B15, B^15
B14, B^14
B13, B^13
B12, B^12
B11, B^11
B10, B^10
B9, B^9
B8, B^8
B7, B^7
B6, B^6
B5, B^5
B4, B^4
B3, B^3
B2, B^2
B1, B^1
B0, B^0
A0/GOE0, A^0
A1, A^1
A2, A^2
A3, A^3
A4, A^4
A5, A^5
A6, A^6
A7, A^7
DIG_00
DIG_01
DIG_02
DIG_03
DIG_04
DIG_05
DIG_06
DIG_07
DIG_08
DIG_09
DIG_10
DIG_11
DIG_12
DIG_13
DIG_14
DIG_15
DIG_16
DIG_17
DIG_18
DIG_19
DIG_20
DIG_21
DIG_22
DIG_23
DIG_24
DIG_25
DIG_26
DIG_27
DIG_28
DIG_29
LC4128V-75TN100C
R65D 0R
R66D 0R
PS_I2C0_SDA_1V8
PS_I2C0_SCL_1V8
BANK 1 @ 3.3V
U4DB
BANK 1
C0, C^0
C1, C^1
C2, C^2
C3, C^3
C4, C^4
C5, C^5
C6, C^6
C7, C^7
C8, C^8
C9, C^9
C10, C^10
C11, C^11
C12, C^12
C13, C^13
C14, C^14
C15, C^15
D15, D^15
D14, D^14
D13, D^13
D12, D^12
D11, D^11
D10, D^10
D9, D^9
D8, D^8
D7, D^7
D6, D^6
D5, D^5
D4, D^4
D3, D^3
D2, D^2
D1, D^1
D0/GOE1, D^0
R61DA 47R DIG_IO_08D
R61DB 47R DIG_IO_10D
R61DC 47R DIG_IO_12D
R61DD 47R DIG_IO_14D
R62DD 47R DIG_IO_06D
R62DC 47R DIG_IO_04D
R62DB 47R DIG_IO_02D
R62DA 47R DIG_IO_00D
R64DD 47R DIG_IO_01D
R64DC 47R DIG_IO_03D
R64DB 47R DIG_IO_05D
R64DA 47R DIG_IO_07D
R63DD 47R DIG_IO_09D
R63DC 47R DIG_IO_11D
R63DB 47R DIG_IO_13D
R63DA 47R DIG_IO_15D
R58DD 47R DIG_IO_17D
R58DC 47R DIG_IO_19D
R58DB 47R DIG_IO_21D
R58DA 47R DIG_IO_23D
R57DA 47R CPLD_DigOut_01D
R57DB 47R DIG_IO_29D
R57DC 47R DIG_IO_27D
R57DD 47R DIG_IO_25D
R59DD 47R CPLD_DigOut_02D
R59DC 47R DIG_IO_28D
R59DB 47R DIG_IO_26D
R59DA 47R DIG_IO_24D
R60DA 47R DIG_IO_16D
R60DB 47R DIG_IO_18D
R60DC 47R DIG_IO_20D
R60DD 47R DIG_IO_22D
LC4128V-75TN100C
X6D
GND
VIN
5V_PER
3V3_PER
DIG_IO_00D
DIG_IO_01D
DIG_IO_02D
DIG_IO_03D
DIG_IO_04D
DIG_IO_05D
DIG_IO_06D
DIG_IO_07D
DIG_IO_08D
DIG_IO_09D
DIG_IO_10D
DIG_IO_11D
DIG_IO_12D
DIG_IO_13D
DIG_IO_14D
DIG_IO_15D
DIG_IO_16D
DIG_IO_17D
DIG_IO_18D
DIG_IO_19D
DIG_IO_20D
DIG_IO_21D
DIG_IO_22D
DIG_IO_23D
DIG_IO_24D
DIG_IO_25D
DIG_IO_26D
DIG_IO_27D
DIG_IO_28D
DIG_IO_29D
DIG_Res_08D
DIG_Res_01D
DIG_Res_00D
DIG_Res_02D
TP54D
TP57D
TP53D
TP58D
CPLD_DigIn_01D
CPLD_DigIn_02D
CPLD_DigOut_01D
CPLD_DigOut_02D
PS_I2C0_shared_SCL
PS_I2C0_shared_SDA
DIG_Res_03D
DIG_Res_04D
DIG_Res_05D
DIG_Res_06D
DIG_Res_07D
TP81D
TP64D
TP67D
TP82D
TP65D
Collective_FLT
PILOT_OUT
PILOT_D_IN
PILOT_IN
HTEC8-150-01-L-DV-K
dedicated inputs of CPLD
U4DG
TP59D
TP60D
TP61D
CPLD_DigIn_01D
CPLD_DigIn_02D
/PILOT_IND
R67D 51R
R68D 51R
R69D 51R
R70D
R72D 51R
R73D 51R
51R
LC4128V-75TN100C
chained programming interface
U4DD
CPLD_TDI
CPLD_TCK
CPLD_TMS
CPLD_TDO
TDI
TCK
TMS
TDO
LC4128V-75TN100C
Clock only for internal timing purposes. The input to output propagation delay time is independent
U4DC
TP62D
CPLD_CLK_2
R71D 33R
TP63D
TP66D
CLK1/I
CLK2/I
CLK3/I
CLK0/I
LC4128V-75TN100C
Power Supply of CPLD
1V8_PER
3V3_PER
GND
C22D 100nF
C23D 100nF
C24D 100nF
C27D 100nF
C28D 100nF
C29D 100nF
C30D 100nF
C31D 100nF
C32D 100nF
C33D 100nF
U4DE
VCCO (Bank0)
VCC
VCCO (Bank1)
LC4128V-75TN100C
U4DF
GND
GND (Bank0)
GND (Bank1)
LC4128V-75TN100C
3V3_PER
D4D
BAT46W-7-F
PILOT_D_IN
(3.3 V)
R74D 0R
R75D 10K
C25D 100nF
U5DA
SN74LVC1G14DRL
/PILOT_IND
C26D 100nF
U5DB
VCC
GND
NC
SN74LVC1G14DRL
Title Digital_Interface.SchDoc
Revision: 04
Design Engineer: A. Geiger & E. Liegmann
Project: UltraZOhm_CarrierBoard.PrjPcb
UltraZohm
www.ultrazohm.com
Date: 11.03.2021
Sheet 8 of 36

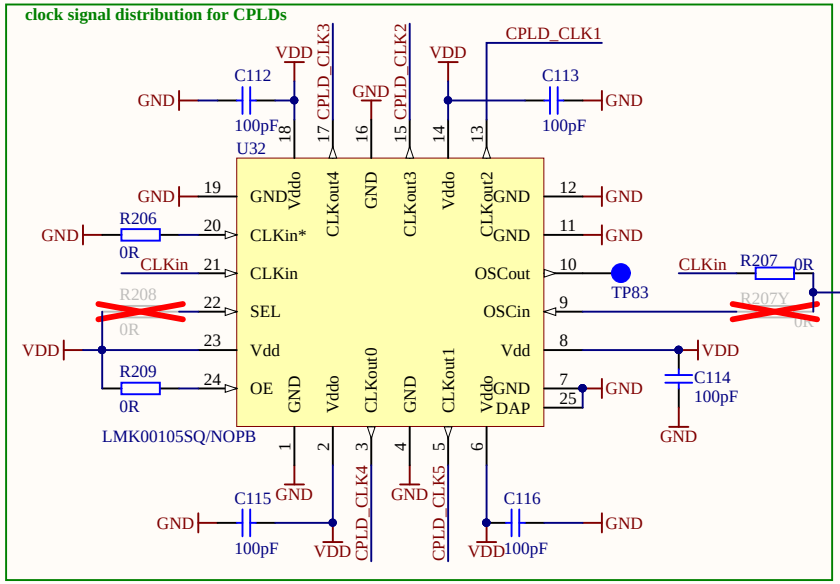

BANK 0 @ 1.8V
U4EA
BANK 0
A8, A^8
A9, A^9
A10, A^10
A11, A^11
A12, A^12
A13, A^13
A14, A^14
A15, A^15
B15, B^15
B14, B^14
B13, B^13
B12, B^12
B11, B^11
B10, B^10
B9, B^9
B8, B^8
B7, B^7
B6, B^6
B5, B^5
B4, B^4
B3, B^3
B2, B^2
B1, B^1
B0, B^0
A0/GOE0, A^0
A1, A^1
A2, A^2
A3, A^3
A4, A^4
A5, A^5
A6, A^6
A7, A^7
DIG_00
DIG_01
DIG_02
DIG_03
DIG_04
DIG_05
DIG_06
DIG_07
DIG_08
DIG_09
DIG_10
DIG_11
DIG_12
DIG_13
DIG_14
DIG_15
DIG_16
DIG_17
DIG_18
DIG_19
DIG_20
DIG_21
DIG_22
DIG_23
DIG_24
DIG_25
DIG_26
DIG_27
DIG_28
DIG_29
LC4128V-75TN100C
R65E 0R
R66E 0R
PS_I2C0_SDA_1V8
PS_I2C0_SCL_1V8
BANK 1 @ 3.3V
U4EB
BANK 1
C0, C^0
C1, C^1
C2, C^2
C3, C^3
C4, C^4
C5, C^5
C6, C^6
C7, C^7
C8, C^8
C9, C^9
C10, C^10
C11, C^11
C12, C^12
C13, C^13
C14, C^14
C15, C^15
D15, D^15
D14, D^14
D13, D^13
D12, D^12
D11, D^11
D10, D^10
D9, D^9
D8, D^8
D7, D^7
D6, D^6
D5, D^5
D4, D^4
D3, D^3
D2, D^2
D1, D^1
D0/GOE1, D^0
R61EA 47R DIG_IO_08E
R61EB 47R DIG_IO_10E
R61EC 47R DIG_IO_12E
R61ED 47R DIG_IO_14E
R62ED 47R DIG_IO_06E
R62EC 47R DIG_IO_04E
R62EB 47R DIG_IO_02E
R62EA 47R DIG_IO_00E
R64ED 47R DIG_IO_01E
R64EC 47R DIG_IO_03E
R64EB 47R DIG_IO_05E
R64EA 47R DIG_IO_07E
R63ED 47R DIG_IO_09E
R63EC 47R DIG_IO_11E
R63EB 47R DIG_IO_13E
R63EA 47R DIG_IO_15E
R58ED 47R DIG_IO_17E
R58EC 47R DIG_IO_19E
R58EB 47R DIG_IO_21E
R58EA 47R DIG_IO_23E
R57EA 47R CPLD_DigOut_01E
R57EB 47R DIG_IO_29E
R57EC 47R DIG_IO_27E
R57ED 47R DIG_IO_25E
R59ED 47R CPLD_DigOut_02E
R59EC 47R DIG_IO_28E
R59EB 47R DIG_IO_26E
R59EA 47R DIG_IO_24E
R60EA 47R DIG_IO_16E
R60EB 47R DIG_IO_18E
R60EC 47R DIG_IO_20E
R60ED 47R DIG_IO_22E
LC4128V-75TN100C
X6E
GND
VIN
5V_PER
3V3_PER
DIG_IO_00E
DIG_IO_01E
DIG_IO_02E
DIG_IO_03E
DIG_IO_04E
DIG_IO_05E
DIG_IO_06E
DIG_IO_07E
DIG_IO_08E
DIG_IO_09E
DIG_IO_10E
DIG_IO_11E
DIG_IO_12E
DIG_IO_13E
DIG_IO_14E
DIG_IO_15E
DIG_IO_16E
DIG_IO_17E
DIG_IO_18E
DIG_IO_19E
DIG_IO_20E
DIG_IO_21E
DIG_IO_22E
DIG_IO_23E
DIG_IO_24E
DIG_IO_25E
DIG_IO_26E
DIG_IO_27E
DIG_IO_28E
DIG_IO_29E
DIG_Res_08E
DIG_Res_00E
DIG_Res_01E
DIG_Res_02E
CPLD_DigIn_01E
CPLD_DigIn_02E
CPLD_DigOut_01E
CPLD_DigOut_02E
PS_I2C0_shared_SCL
PS_I2C0_shared_SDA
DIG_Res_03E
DIG_Res_04E
DIG_Res_05E
DIG_Res_06E
DIG_Res_07E
Collective_FLT
PILOT_OUT
PILOT_D_IN5
PILOT_IN
TP53E
TP58E
TP82E
TP65E
HTEC8-150-01-L-DV-K
dedicated inputs of CPLD
U4EG
TP59E
TP60E
TP61E
CPLD_DigIn_01E
CPLD_DigIn_02E
/PILOT_INE
R67E 51R
R68E 51R
R69E 51R
R70E
R72E 51R
R73E 51R
51R
LC4128V-75TN100C
chained programming interface
U4ED
CPLD_TDI
CPLD_TCK
CPLD_TMS
CPLD_TDO
TDI
TCK
TMS
TDO
LC4128V-75TN100C
Clock only for internal timing purposes. The input to output propagation delay time is independent
U4EC
TP62E
CPLD_CLK_2
TP63E
TP66E
R71E 33R
CLK1/I
CLK2/I
CLK3/I
CLK0/I
LC4128V-75TN100C
Power Supply of CPLD
1V8_PER
3V3_PER
GND
C22E 100nF
C23E 100nF
C24E 100nF
C27E 100nF
C28E 100nF
C29E 100nF
C30E 100nF
C31E 100nF
C32E 100nF
C33E 100nF
U4EE
VCCO (Bank0)
VCC
VCCO (Bank1)
LC4128V-75TN100C
U4EF
GND
GND (Bank0)
GND (Bank1)
LC4128V-75TN100C
3V3_PER
D4E
BAT46W-7-F
PILOT_D_IN5
(3.3 V)
R74E 0R
R75E 10K
C25E 100nF
U5EA
SN74LVC1G14DRL
/PILOT_INE
C26E 100nF
U5EB
VCC
GND
NC
SN74LVC1G14DRL
Title Digital_Interface.SchDoc
Revision: 04
Design Engineer: A. Geiger & E. Liegmann
Project: UltraZOhm_CarrierBoard.PrjPcb
UltraZohm
www.ultrazohm.com
Date: 11.03.2021
Sheet 8 of 36



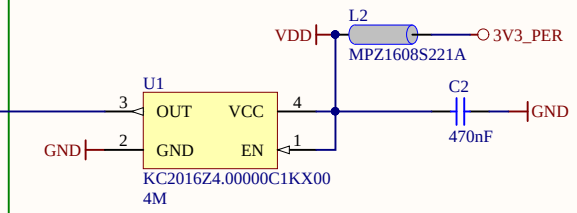
Title Collective_FAULT_logic.SchDoc		UltraZohm www.ultrazohm.com
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 10 of 36

CPLD_TDI[1..5]
CPLD_TDO[1..5]
CPLD_TCK
CPLD_TMS
CPLD_CLK[1..5]

clock signal distribution for CPLDs

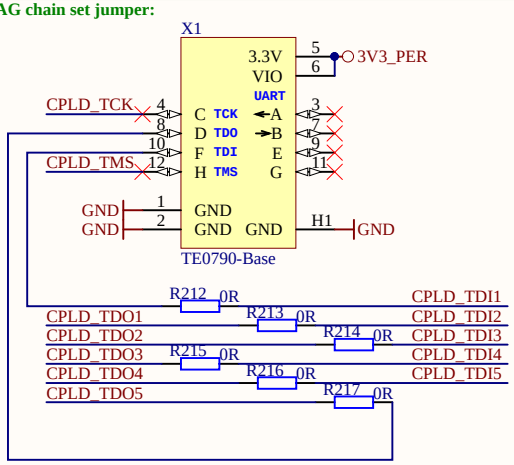


clock signal generation for CPLDs

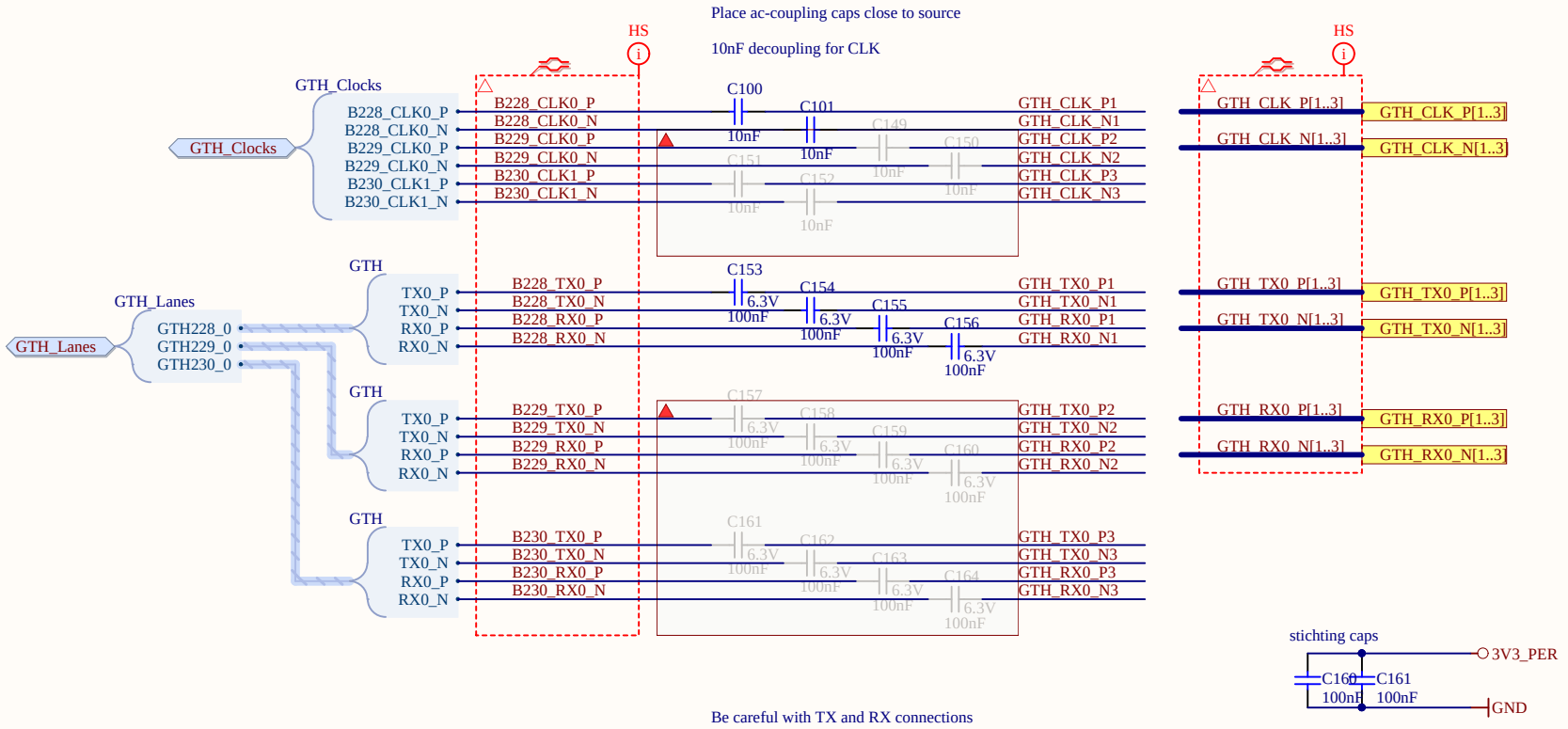


for JTAG chain set jumper:

1 - 2
3 - 4
5 - 6
7 - 8
9 - 10
11 - 12

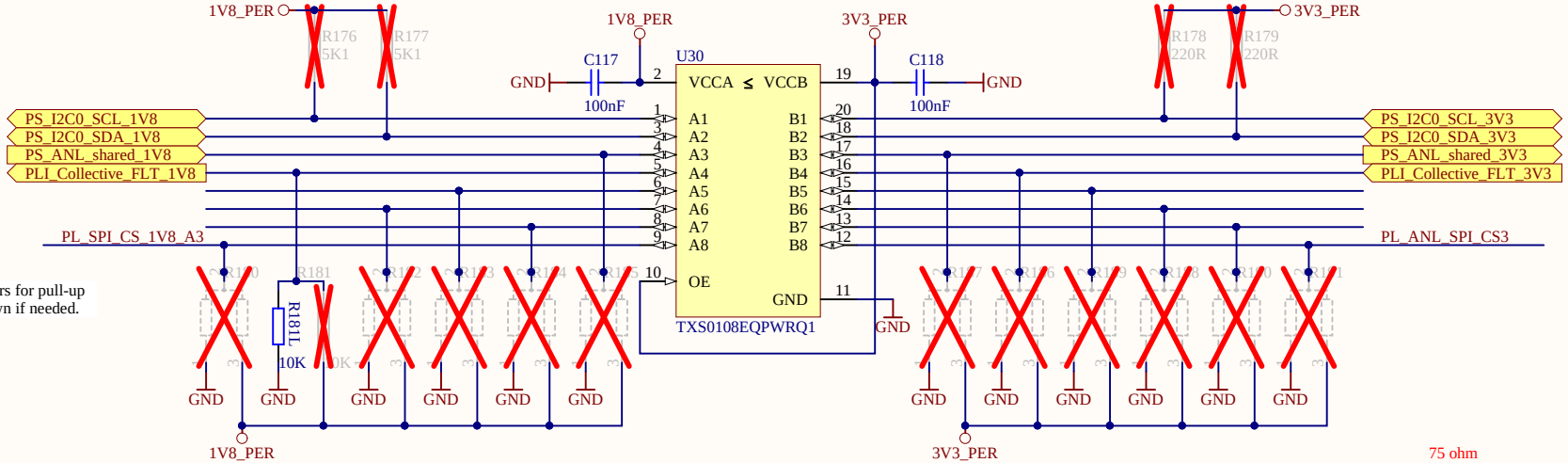


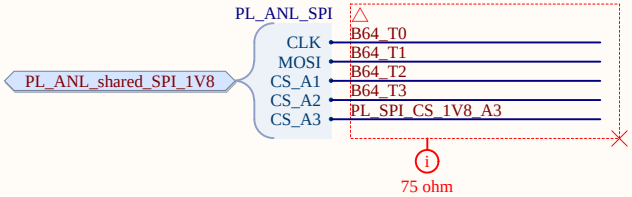
Title CPLD_Programming.SchDoc		UltraZohm www.ultrazohm.com
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 13 of 36



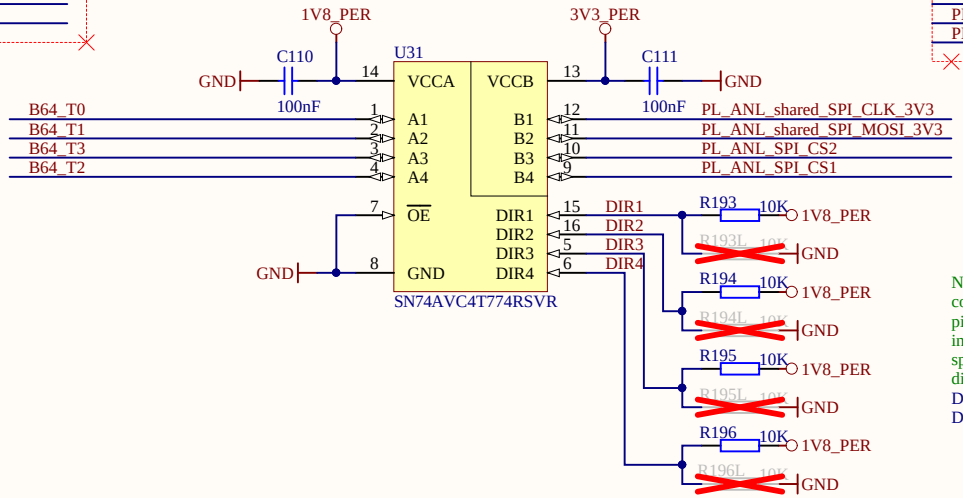
Title GTH.SchDoc		UltraZohm www.ultrazohm.com
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	Date: 11.03.2021
Project: UltraZOhm_CarrierBoard.PrjPcb		Sheet 14 of 36

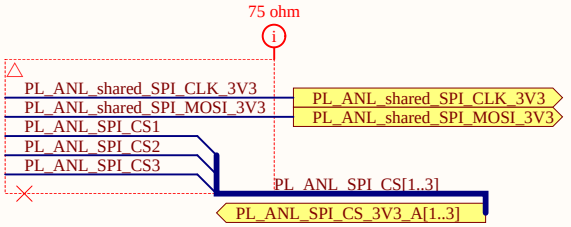
Bidirectional Level Shifting 1.8V to 3.3V





Unidirectional level Shifting 1.8V to 3.3V





Note: by the correct configuration of the DIR pins the IO ports act as input and output as specified by the port direction
DIR = High = A->B
DIR = Low = A<-B

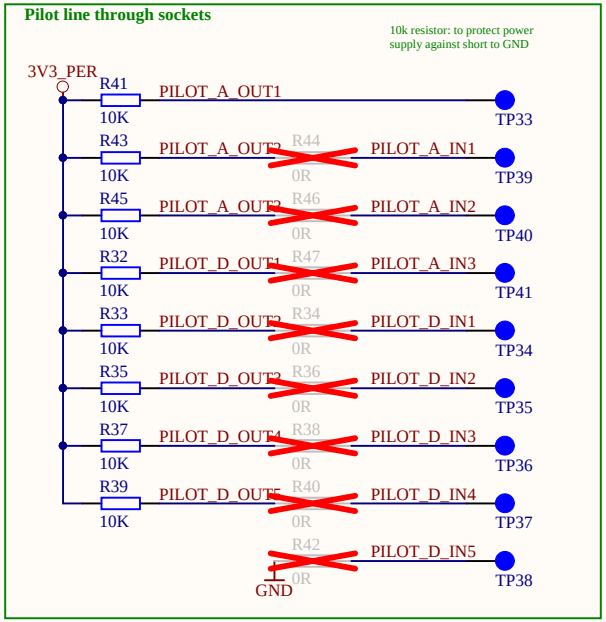
Title LevelShifting.SchDoc		**UltraZohm**	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 11 of 36	

PILOT_D_OUT[1..5] PILOT_D_OUT[1..5]

PILOT_D_IN[1..5] PILOT_D_IN[1..5]

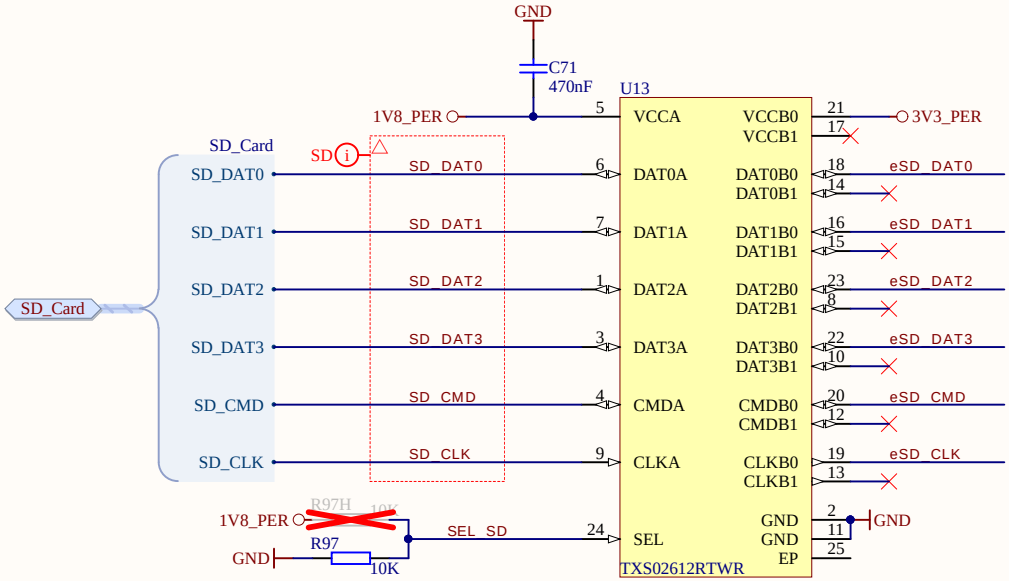
PILOT_A_OUT[1..3] PILOT_A_OUT[1..3]

PILOT_A_IN[1..3] PILOT_A_IN[1..3]



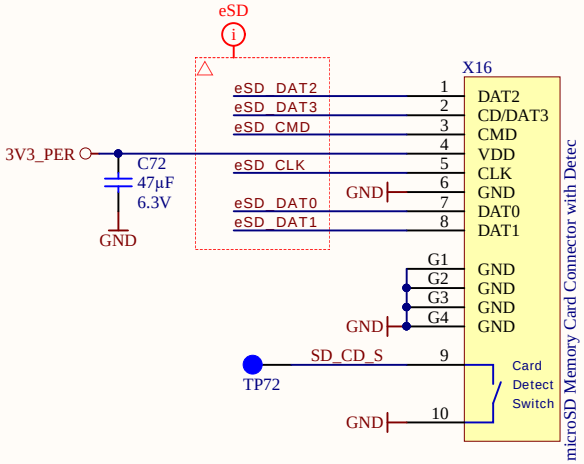
Title Pilot_Line.SchDoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 12 of 36	

Bidirectional Level Shifting 1.8V to 3.3V



SEL_SD on DGND to enable B0

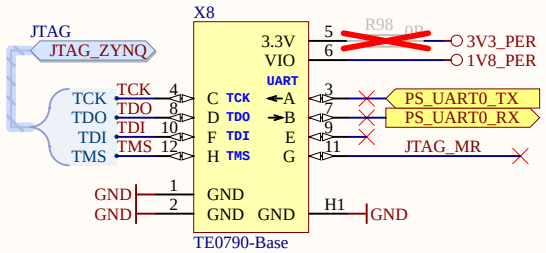
SD Card Connector



Title SD_Card.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 31 of 36	

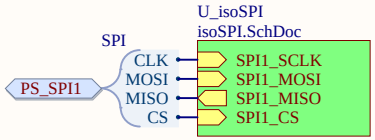
JTAG-Interface

JTAG/UART header ('XMOD FTDI JTAG Adapter'-compatible) for access to MPSoC module



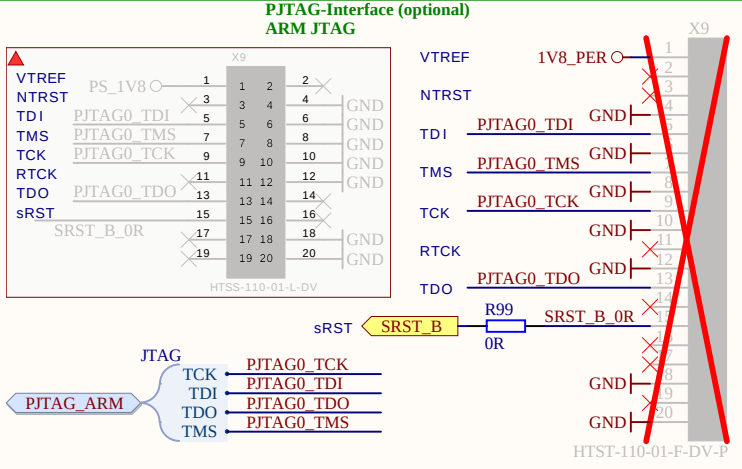
XMOD-FT2232H header: JTAG and UART

Isolated SPI-Interface

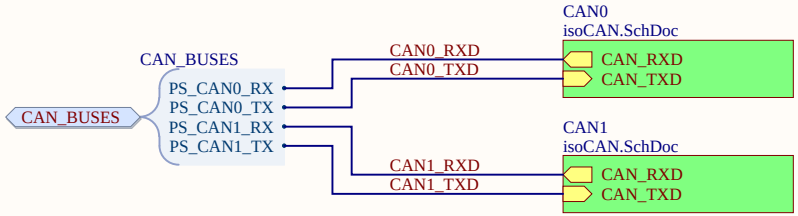


PJTAG-Interface (optional)

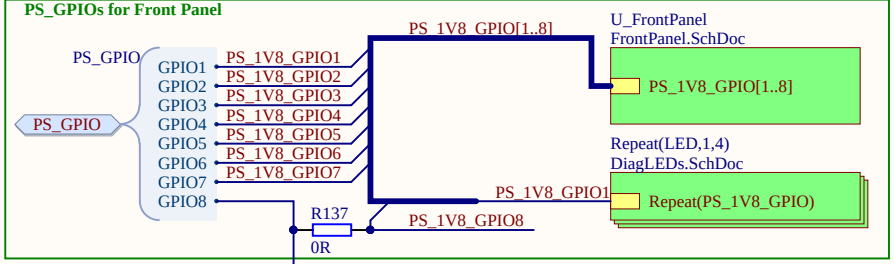
ARM JTAG



2x Isolated CAN-Interface

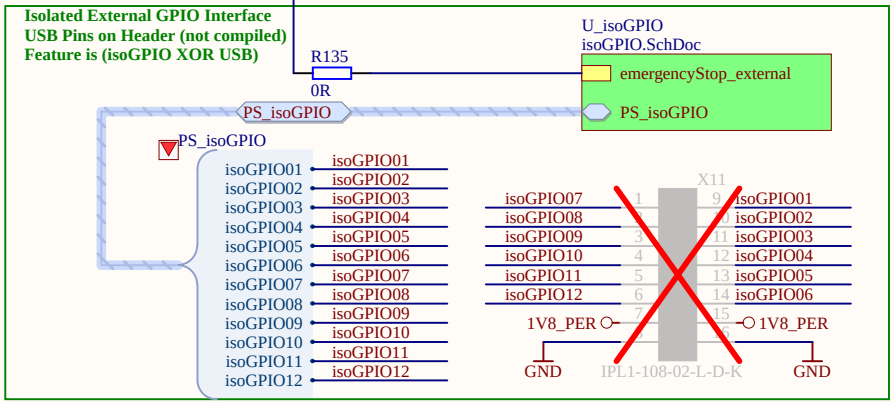


PS_GPIOs for Front Panel



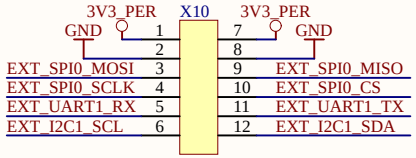
Isolated External GPIO Interface

USB Pins on Header (not compiled)
Feature is (isoGPIO XOR USB)



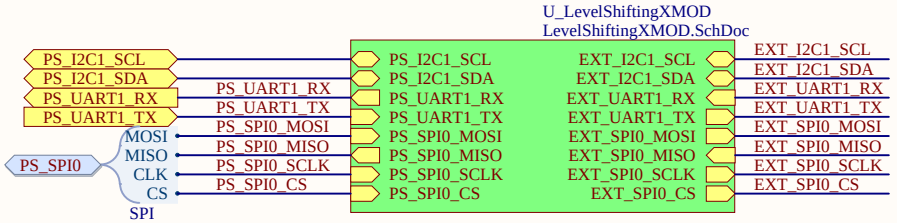
SPI, UART, I2C-Interface (from Processor System)

SPI, UART and I2C Connector @ 3.3V level

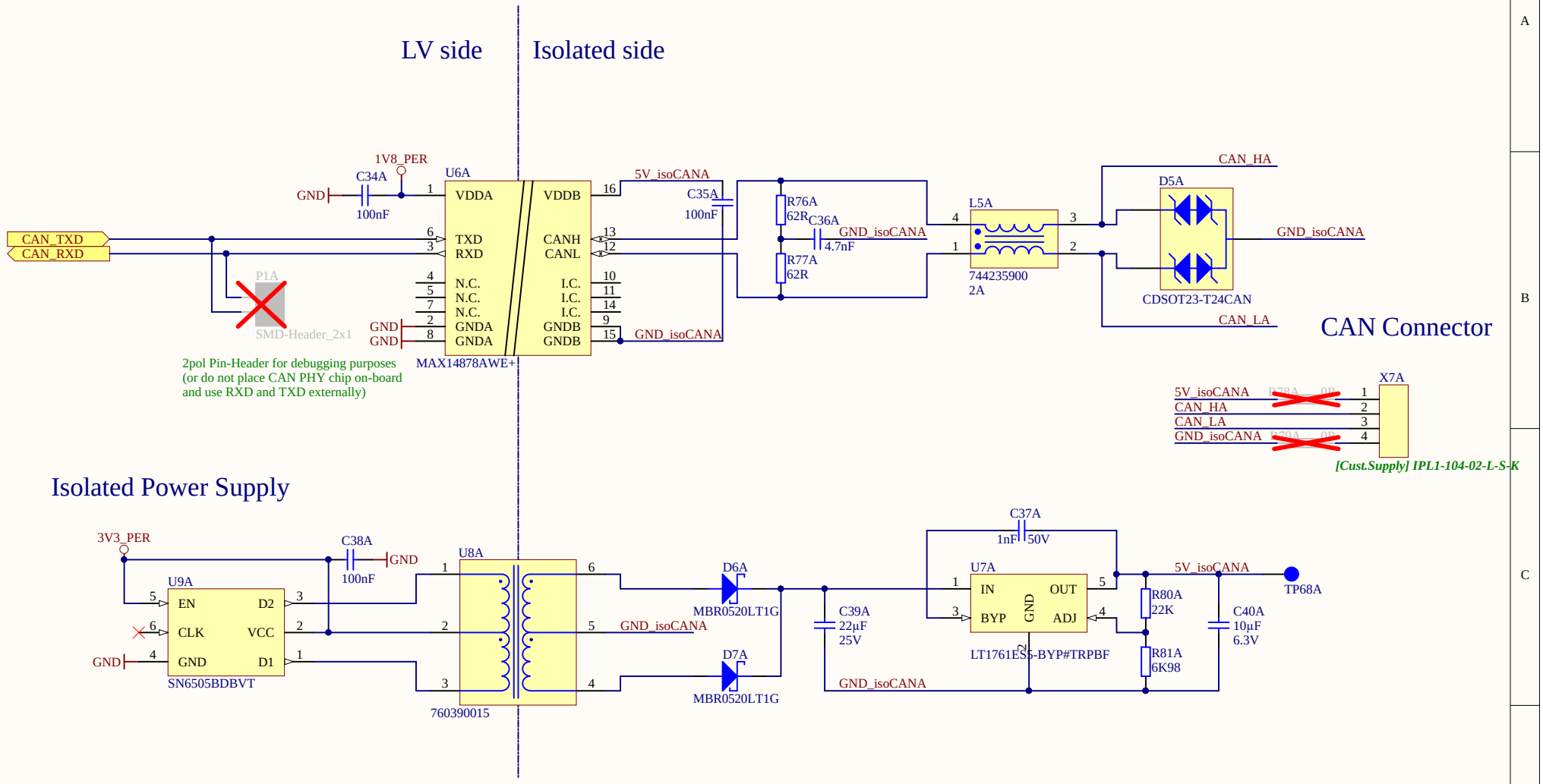


[Cust.Supply] IPL1-106-02-L-D-K

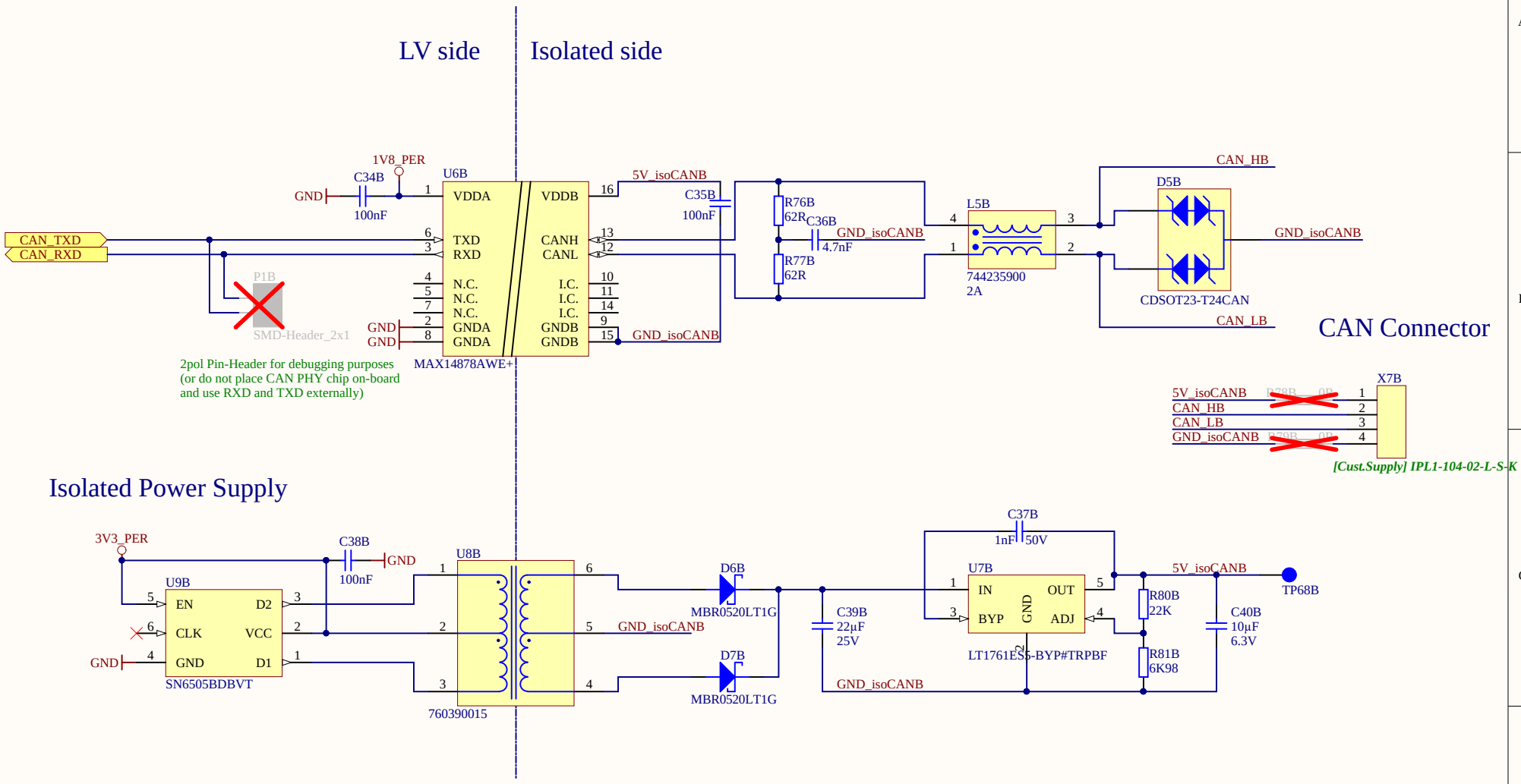
Bidirectional Level Shifting 1.8V to 3.3V



Title XMOD.SchDoc		**UltraZohm**	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 15 of 36	

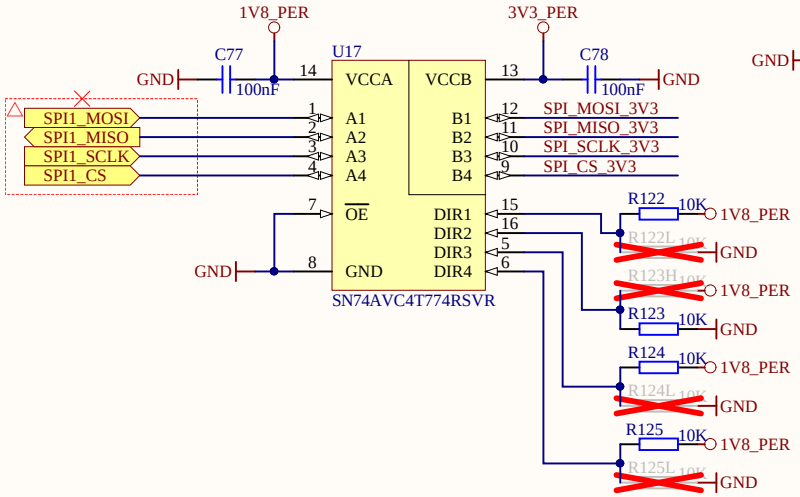


Title isoCAN.SchDoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 16 of 36	

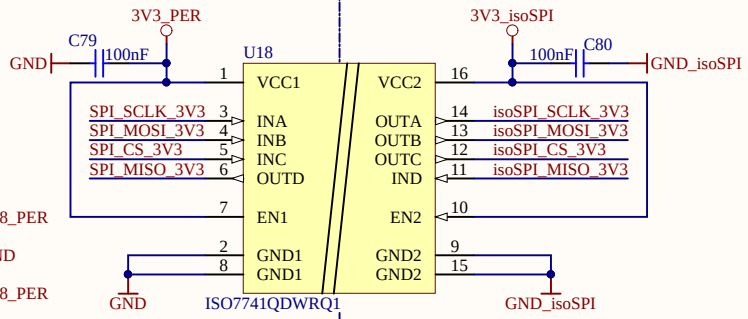


Title isoCAN.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	Sheet 16 of 36

Level Shifting 1.8V to 3.3V



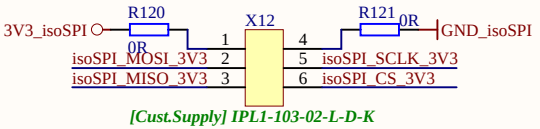
LV side / Isolated side



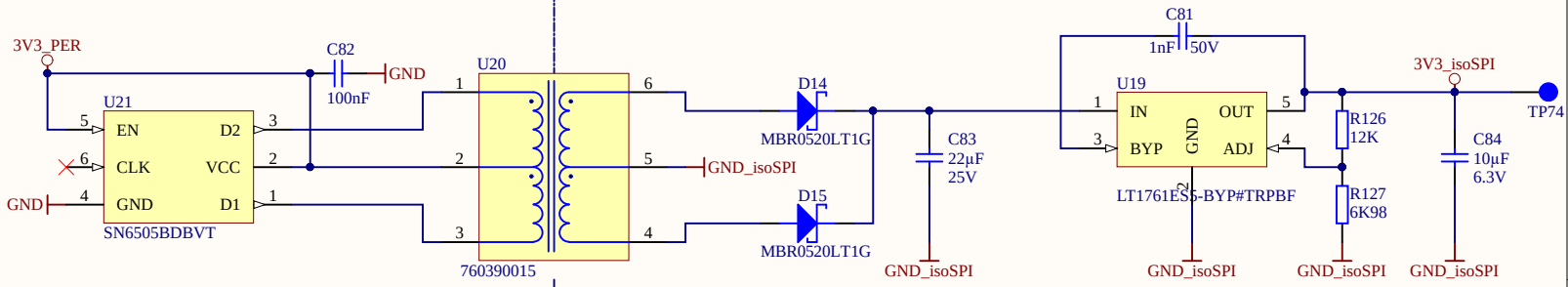
take ADUM4402 if SoC acts as SPI slave

alternative pin-compatible part: Texas Instruments ISO7741DW

SPI Connector

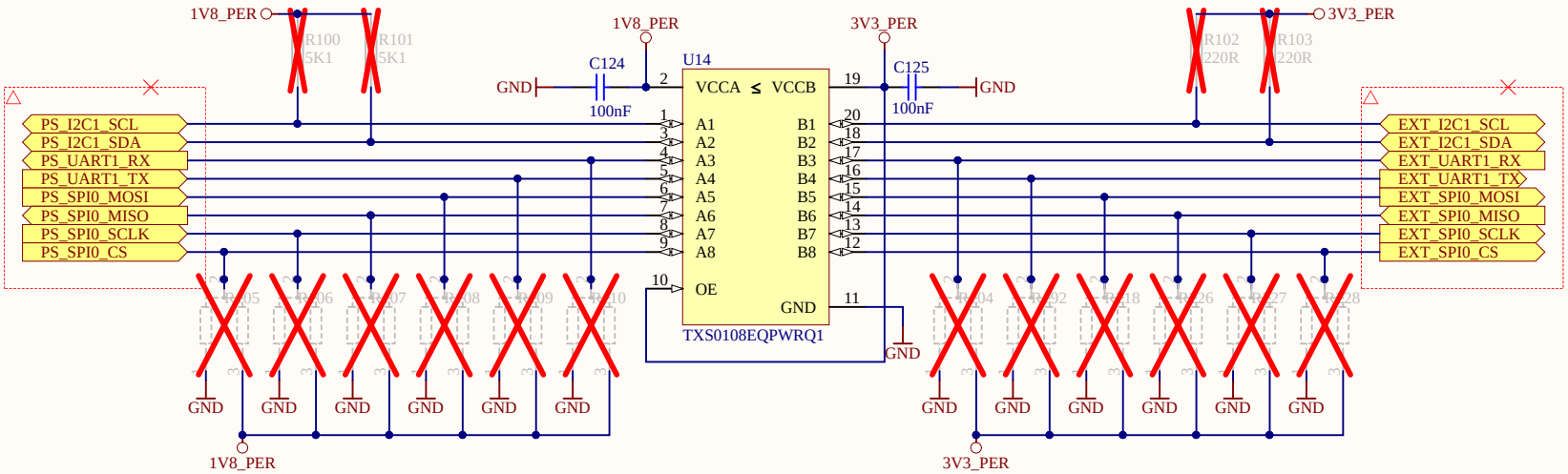


Isolated Power Supply

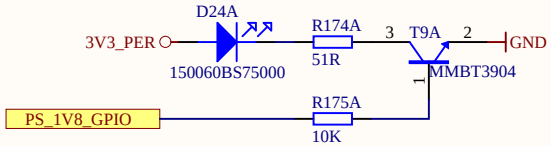


Title isoSPI.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 17 of 36	

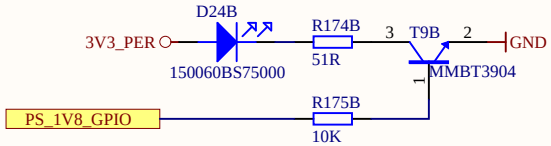
Bidirectional Level Shifting 1.8V to 3.3V



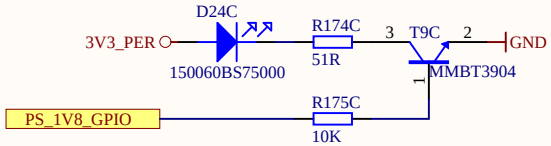
Title LevelShiftingXMOD.SchDoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 23 of 36	



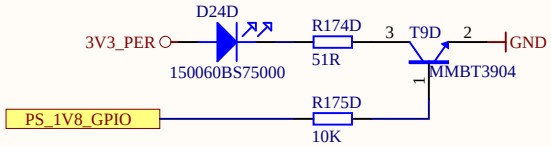
Title DiagLEDs.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 22 of 36	



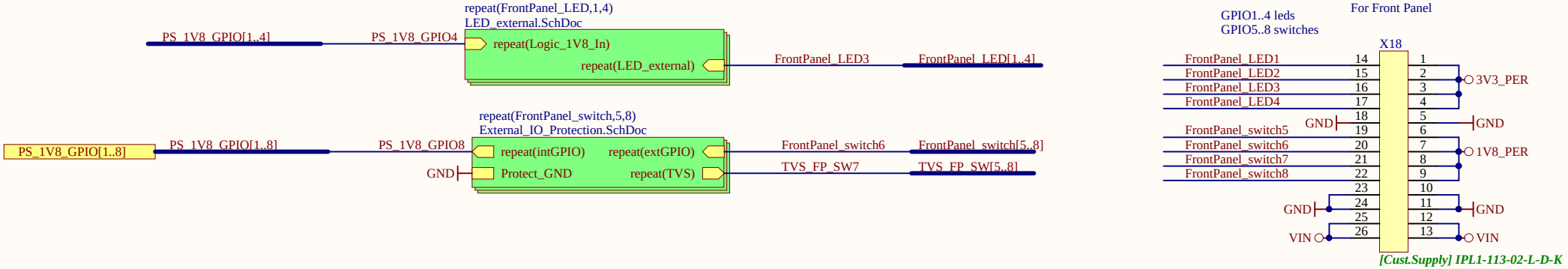
Title DiagLEDs.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 22 of 36	

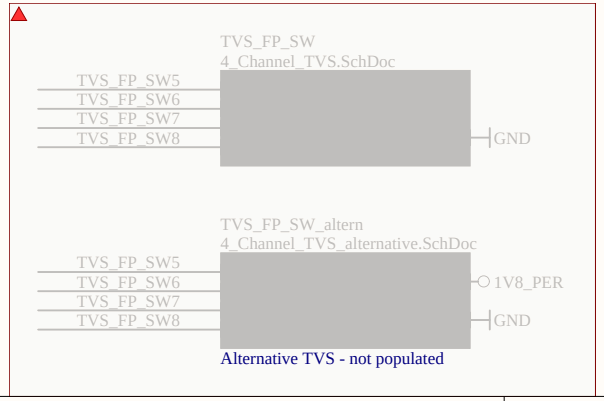


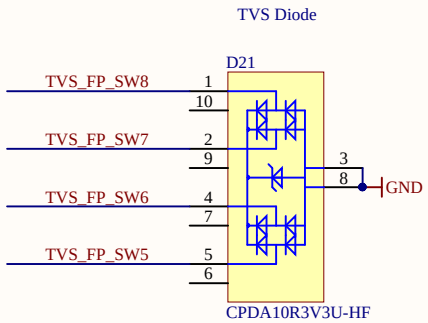
Title DiagLEDs.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 22 of 36	

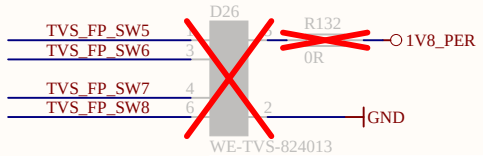


Title DiagLEDs.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 22 of 36	



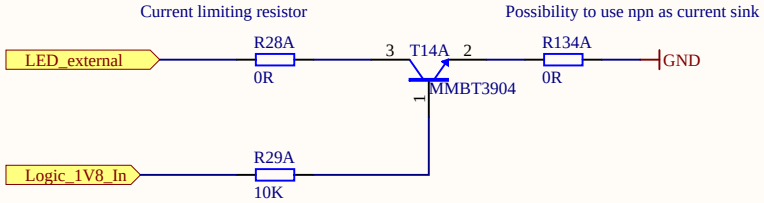






pin-compatible unidirectional alternative:
LittleFuse SP3019
ST ESDA5V3SC6Y
only change: pin 5 needs to be NC

Title FrontPanel.SchDoc		UltraZohm www.ultrazohm.com
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	Date: 11.03.2021
Project: UltraZOhm_CarrierBoard.PrjPcb		Sheet 24 of 36



Two methods to drive the external LED

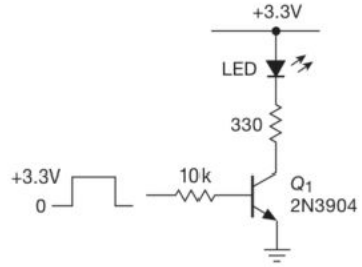


Figure 2.9. Driving an LED from a "logic-level" input signal, using an *npn* saturated switch and series current-limiting resistor.

B. Transistor current source

Happily, it is possible to make a very good current source with a transistor (Figure 2.31). It works like this: applying V_B to the base, with $V_B > 0.6$ V, ensures that the emitter is always conducting:

$$V_E = V_B - 0.6 \text{ volts}.$$

So

$$I_E = V_E/R_E = (V_B - 0.6 \text{ volts})/R_E.$$

But, since $I_E \approx I_C$ for large beta,

$$I_C \approx (V_B - 0.6 \text{ volts})/R_E, \qquad (2.5)$$

independent of V_C, as long as the transistor is not saturated ($V_C \gtrsim V_E + 0.2$ volts).

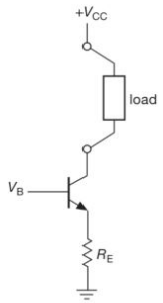
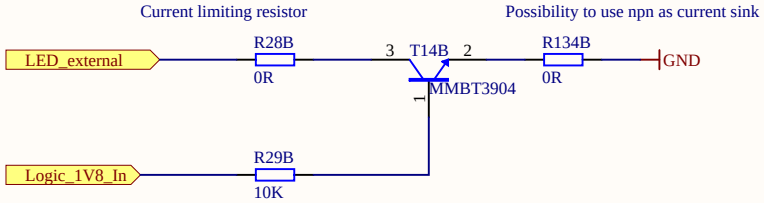
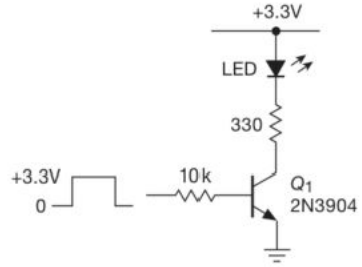


Figure 2.31. Transistor current source: basic concept.

Title LED_external.SchDoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 25 of 36	



Two methods to drive the external LED



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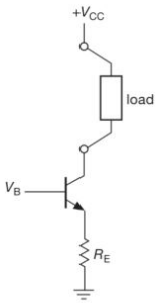

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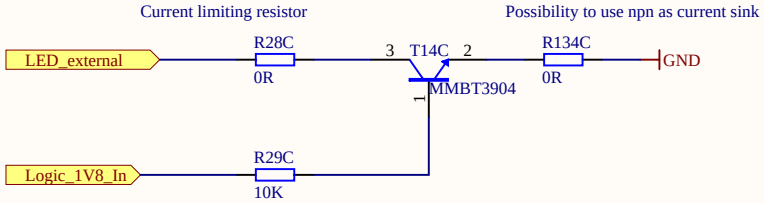
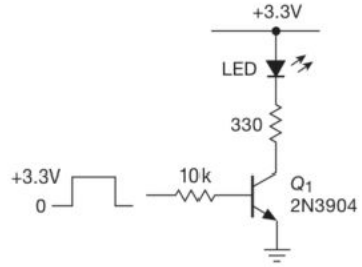
Title LED_external.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 25 of 36	



Two methods to drive the external LED



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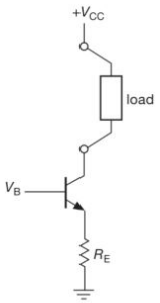
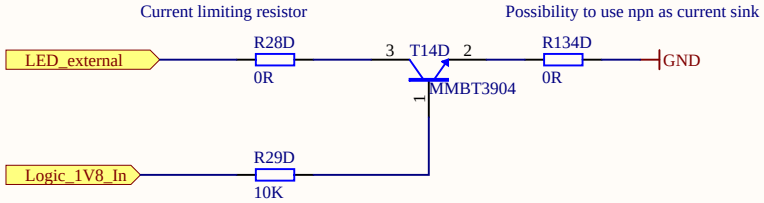
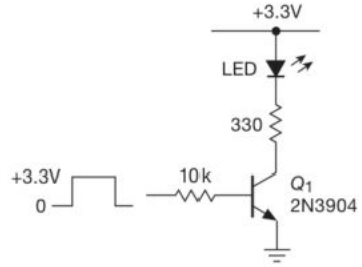


Figure 2.31. Transistor current source: basic concept.

Title LED_external.SchDoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 25 of 36	



Two methods to drive the external LED



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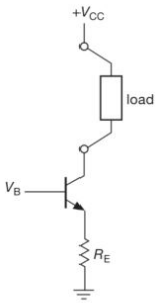
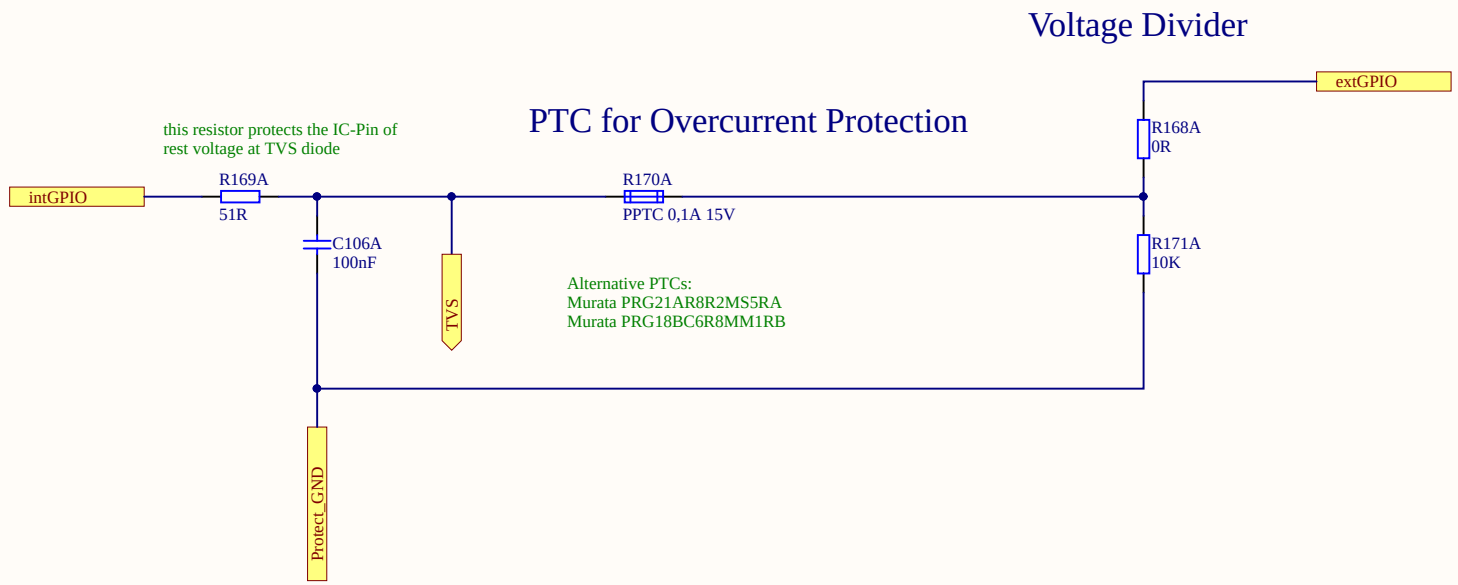
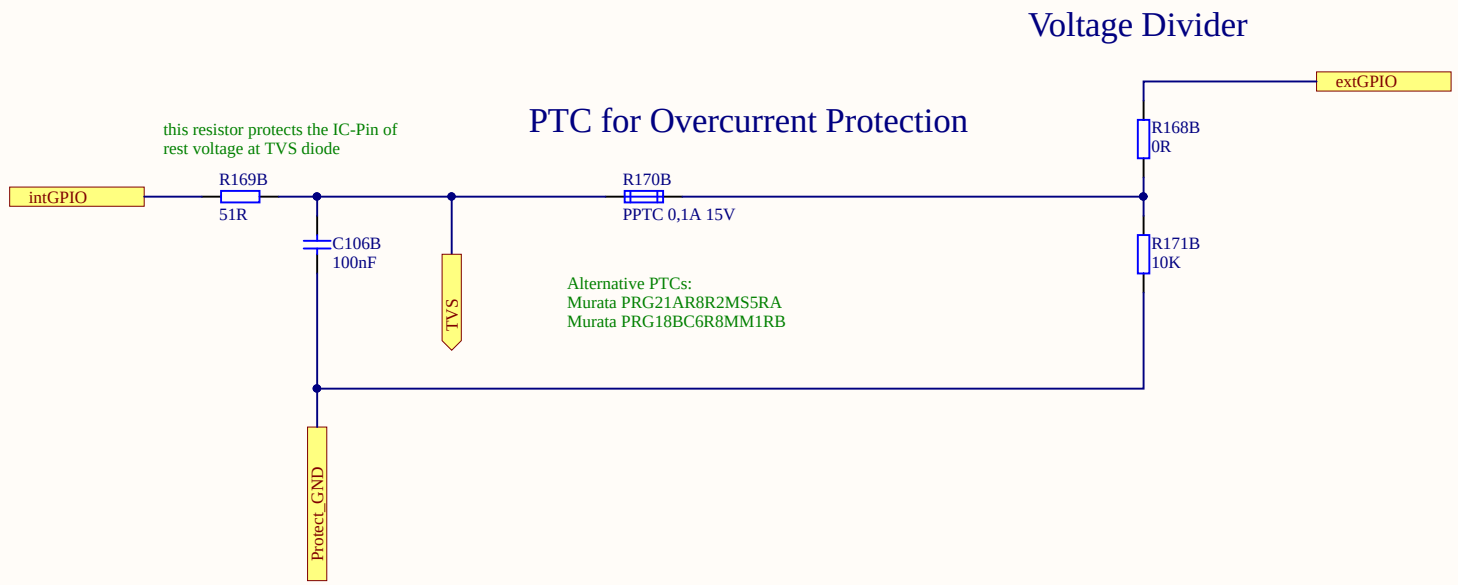


Figure 2.31. Transistor current source: basic concept.

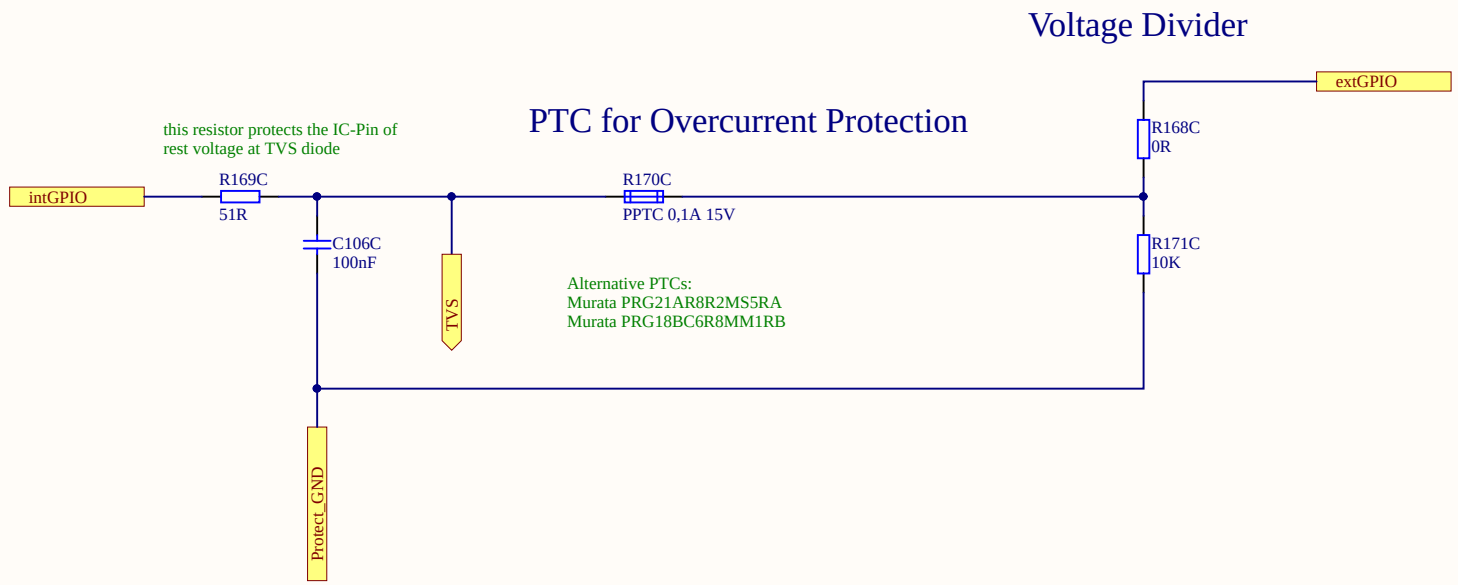
Title LED_external.SchDoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 25 of 36	



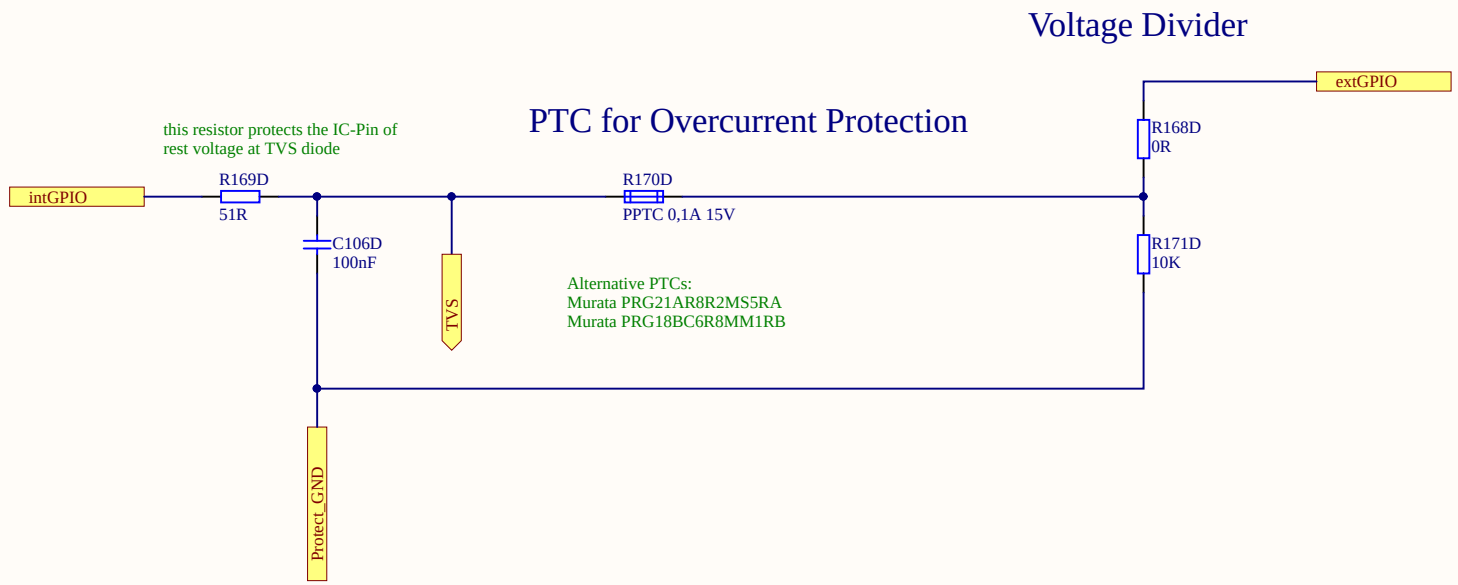
Title External_IO_Protection.SchDoc		UltraZohm www.ultrazohm.com
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 20 of 36



Title External_IO_Protection.SchDoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 20 of 36	



Title External_IO_Protection.SchDoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 20 of 36	

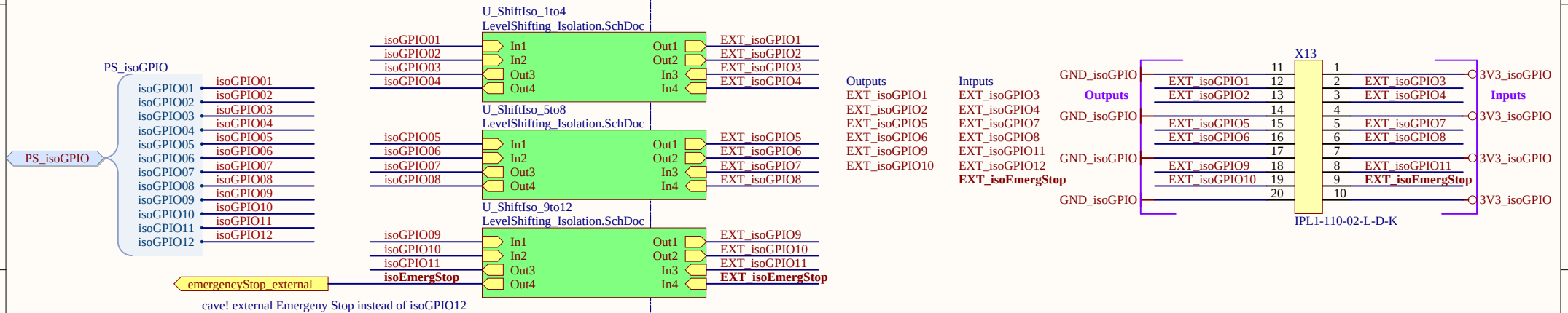


Title External_IO_Protection.SchDoc		UltraZohm www.ultrazohm.com
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 20 of 36

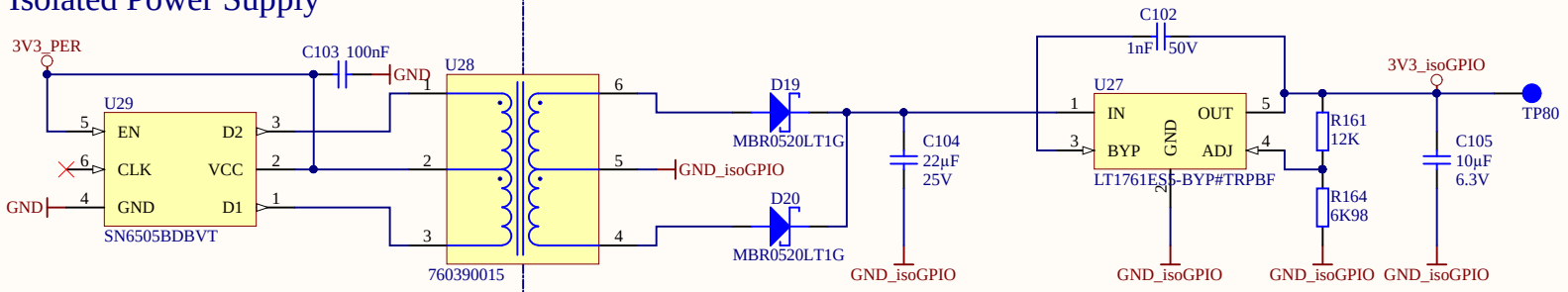
LV side

Bidirectional Level Shifting 1.8V to 3.3V

Isolated & protected side



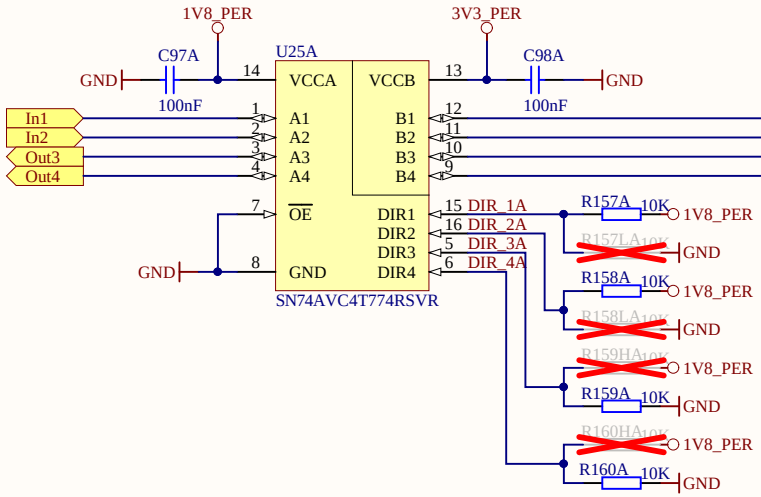
Isolated Power Supply



Title isoGPIO.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	Sheet 18 of 36

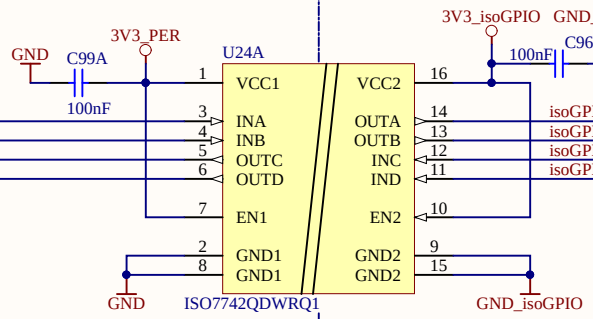
IO Protection with TVS-Diode and PTC-Resistor

Unidirectional level Shifting 1.8V to 3.3V

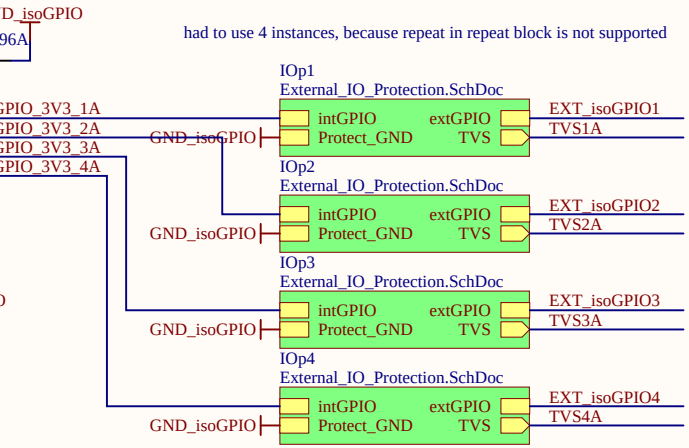


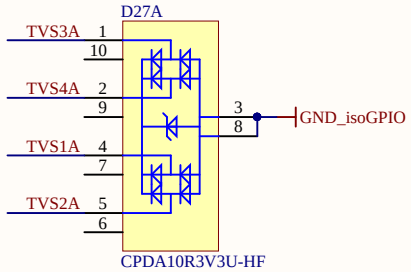
DIR = High = A->B
DIR = Low = A<-B

LV side

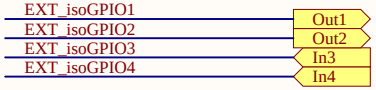


Isolated side

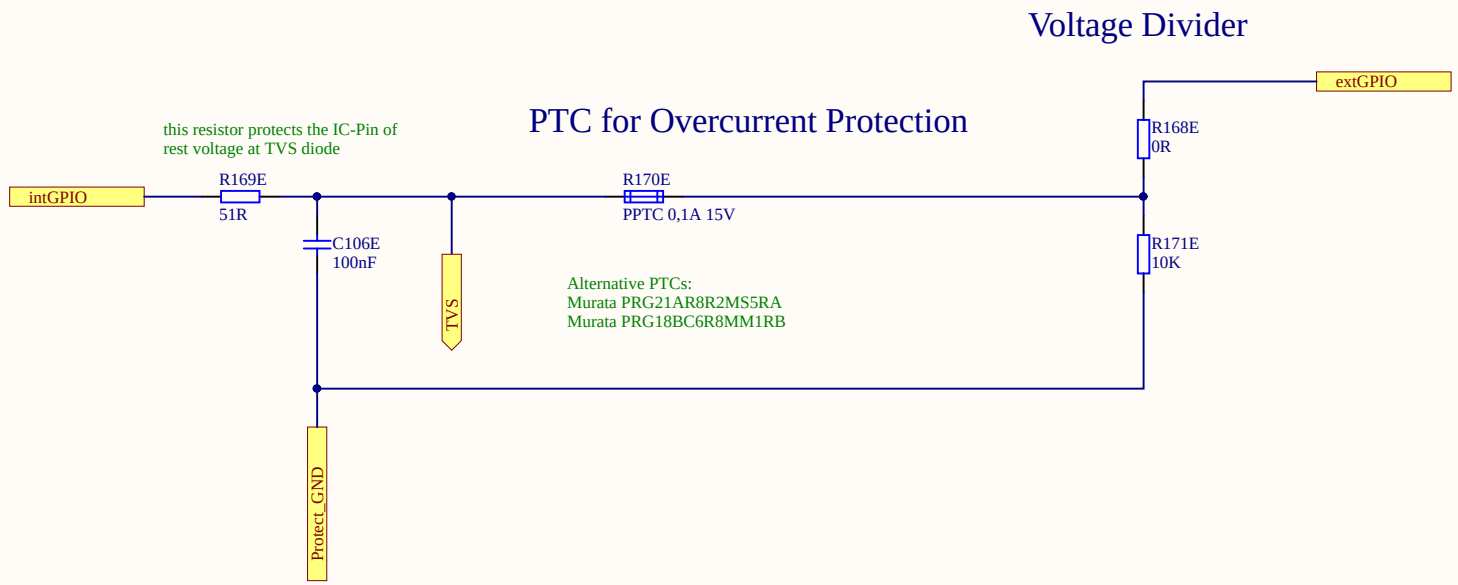




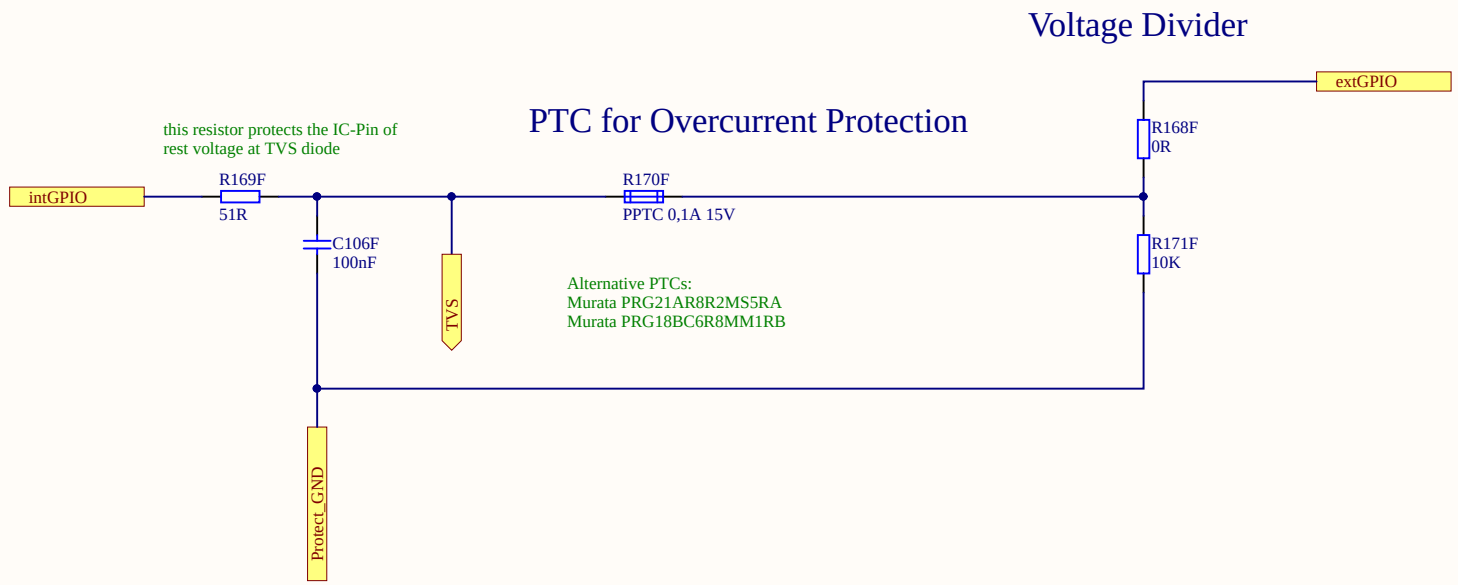
Inputs & Outputs isolated & protected



Title LevelShifting_Isolation.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	Sheet 19 of 36



Title External_IO_Protection.SchDoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 20 of 36	



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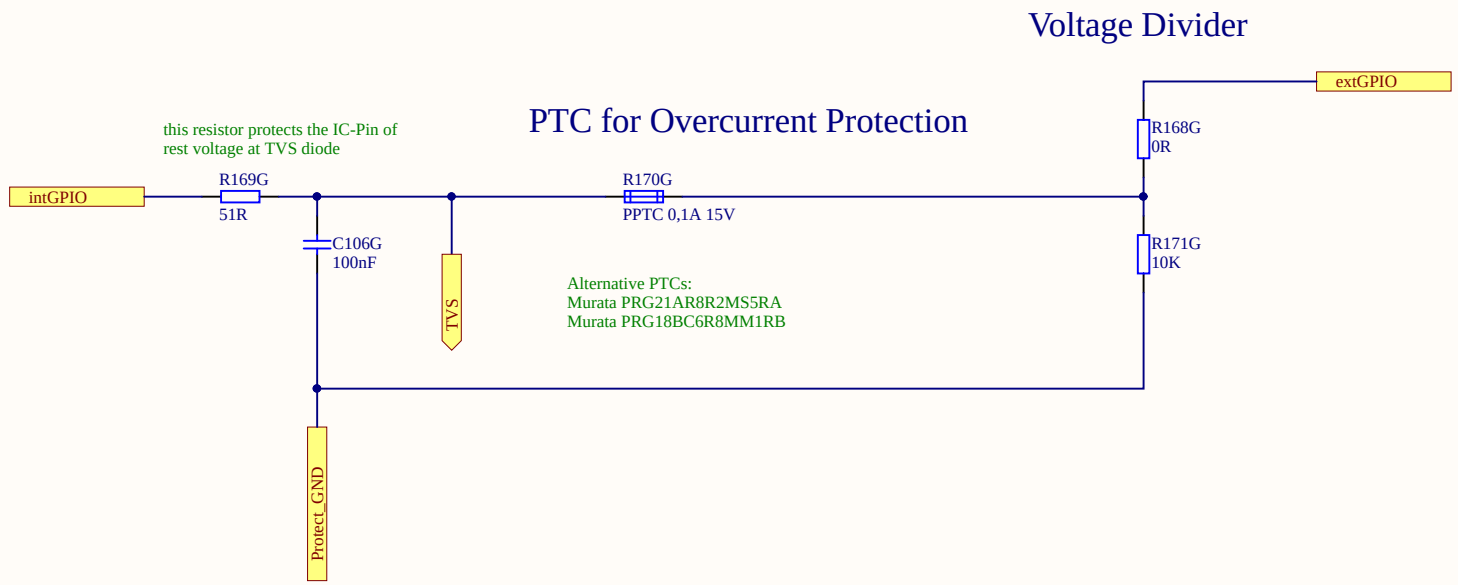
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 20 of 36	



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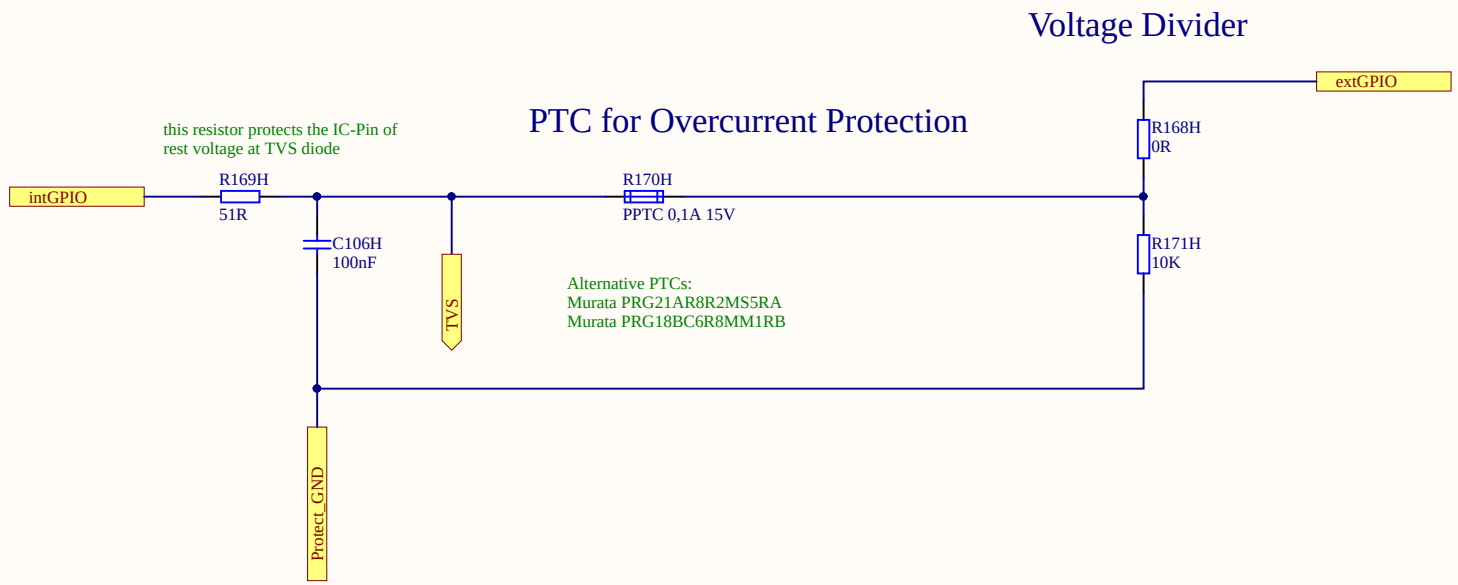

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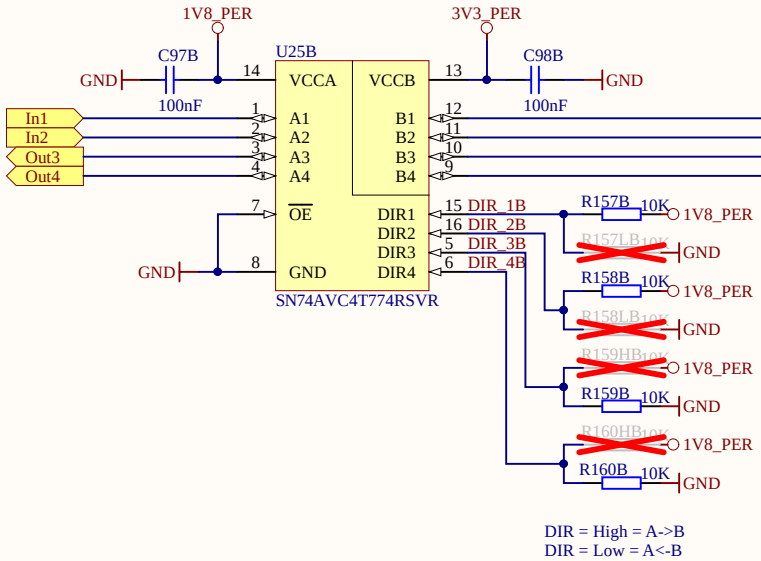
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 20 of 36	

IO Protection with TVS-Diode and PTC-Resistor

Unidirectional level Shifting 1.8V to 3.3V



DIR = High = A->B
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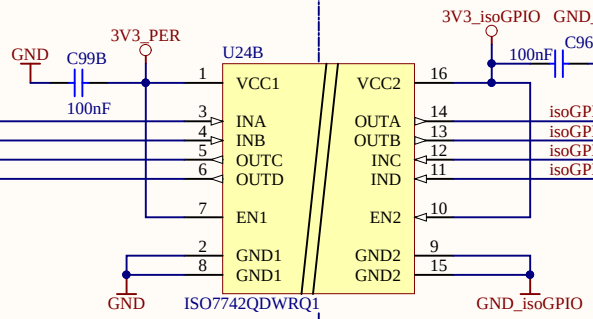
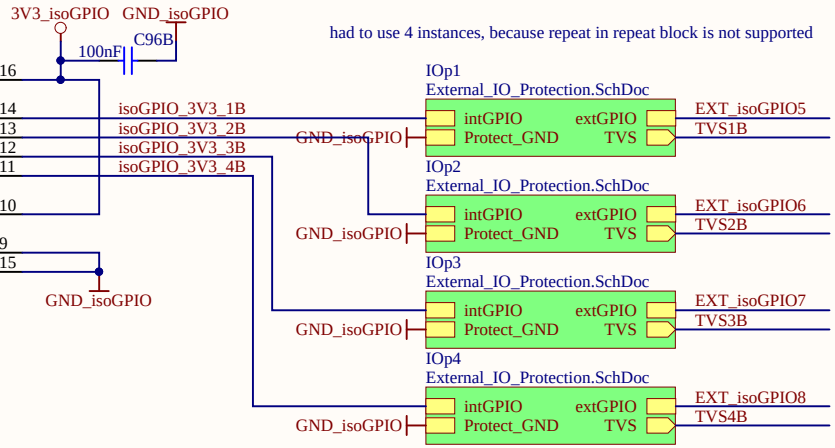
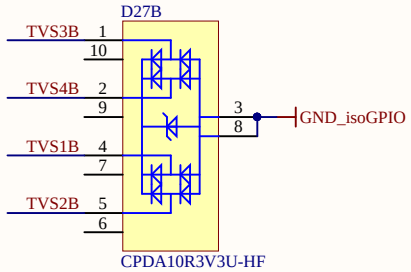
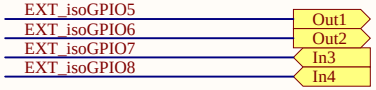


Isolated side

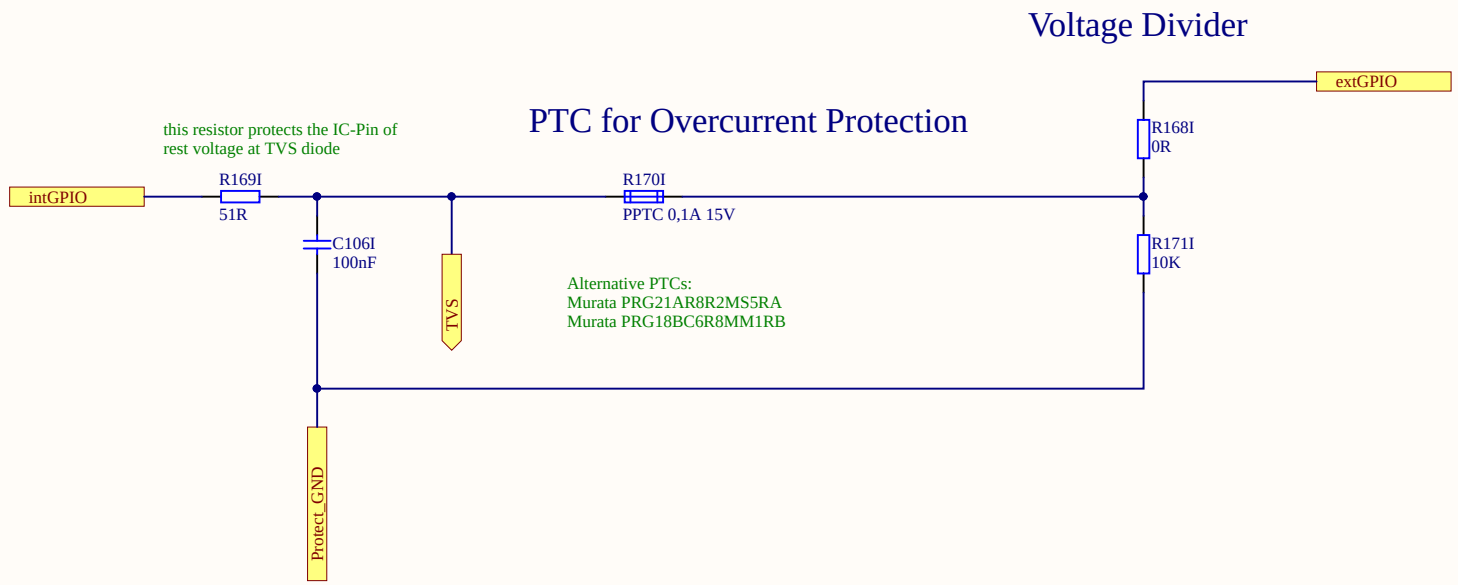




Inputs & Outputs isolated & protected



Title LevelShifting_Isolation.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	Sheet 19 of 36



Title External_IO_Protection.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
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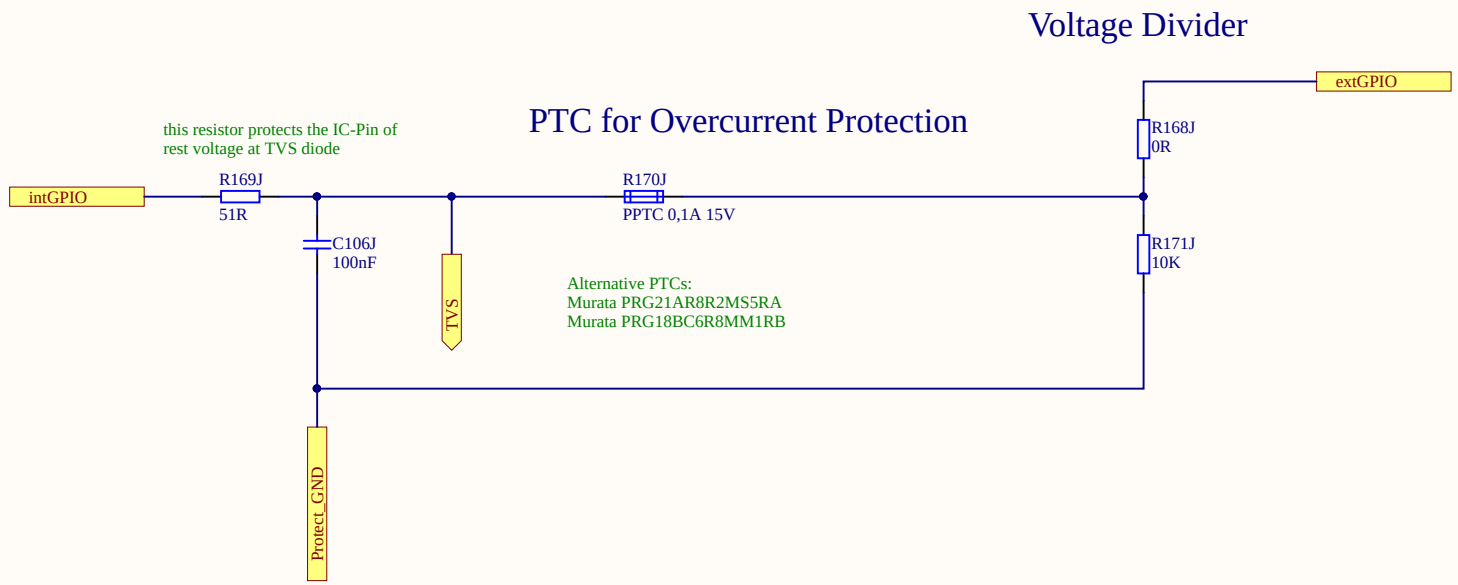

Title External_IO_Protection.SchDoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
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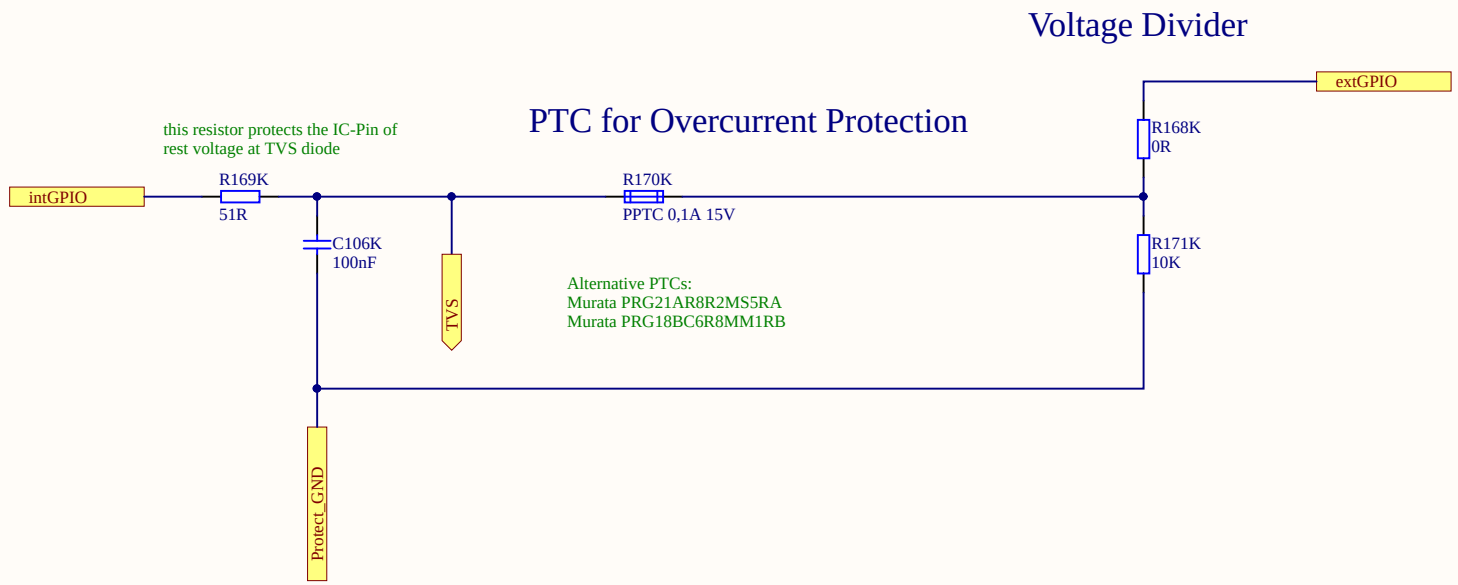

Title External_IO_Protection.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
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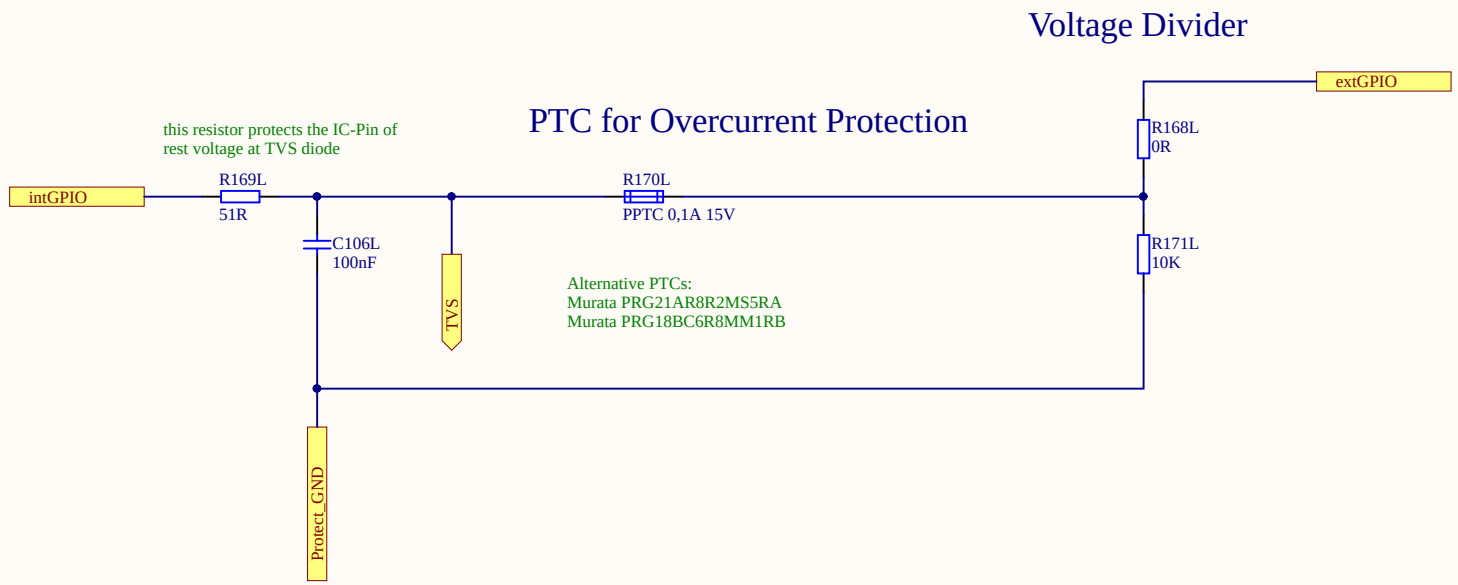

Title External_IO_Protection.SchDoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
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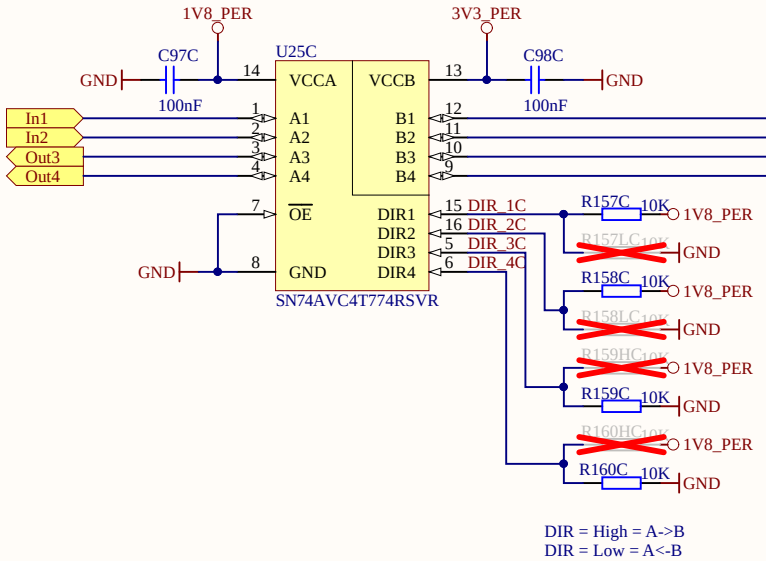
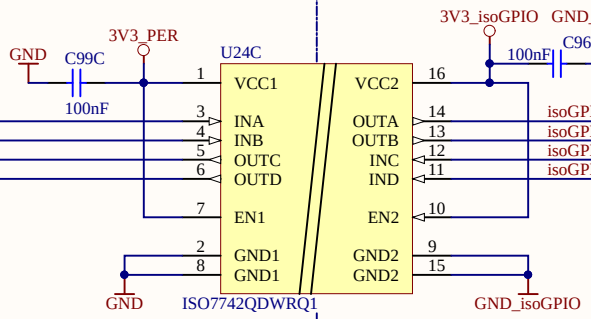
IO Protection with TVS-Diode and PTC-Resistor

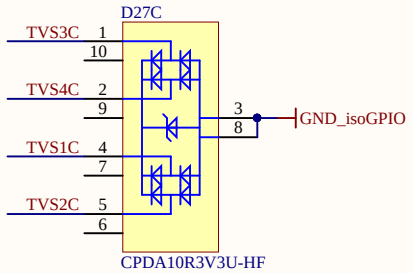
Unidirectional level Shifting 1.8V to 3.3V



LV side

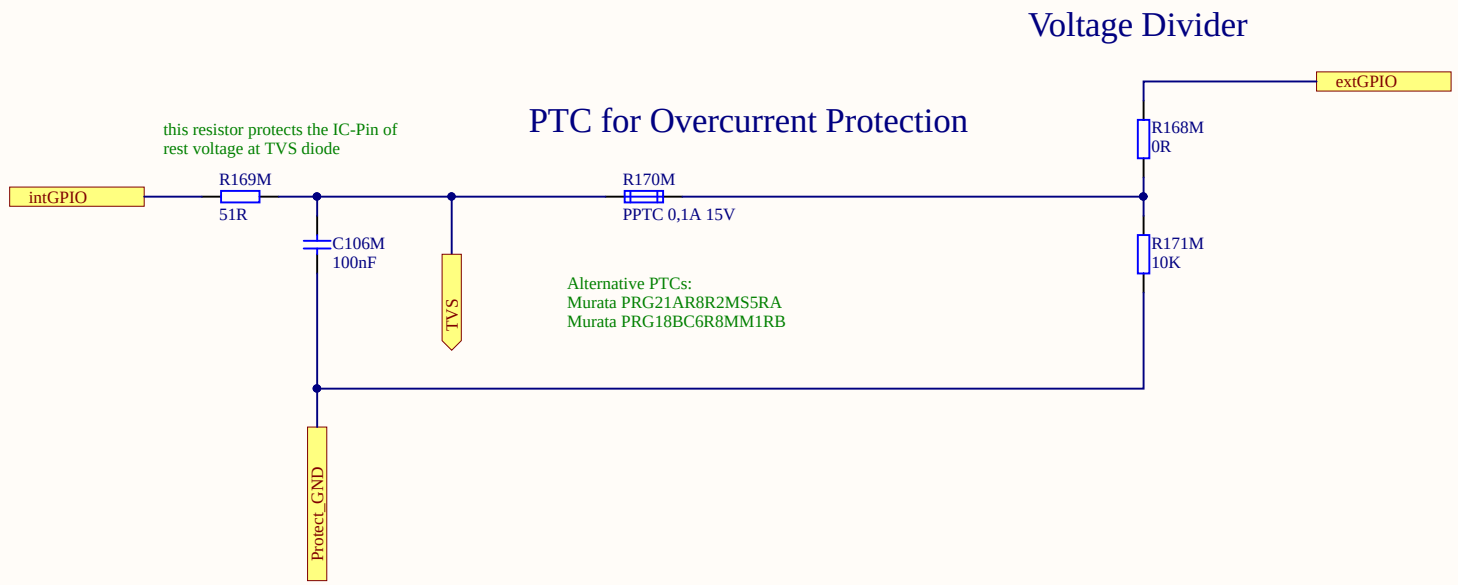


Isolated side

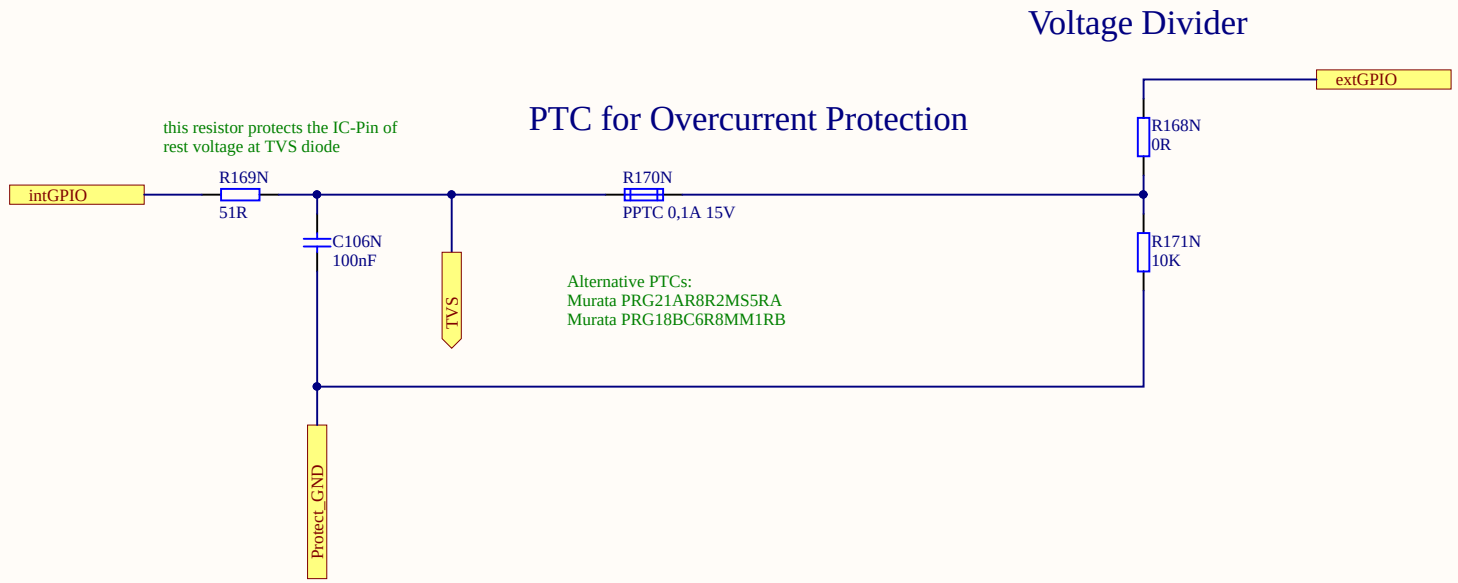


Inputs & Outputs isolated & protected

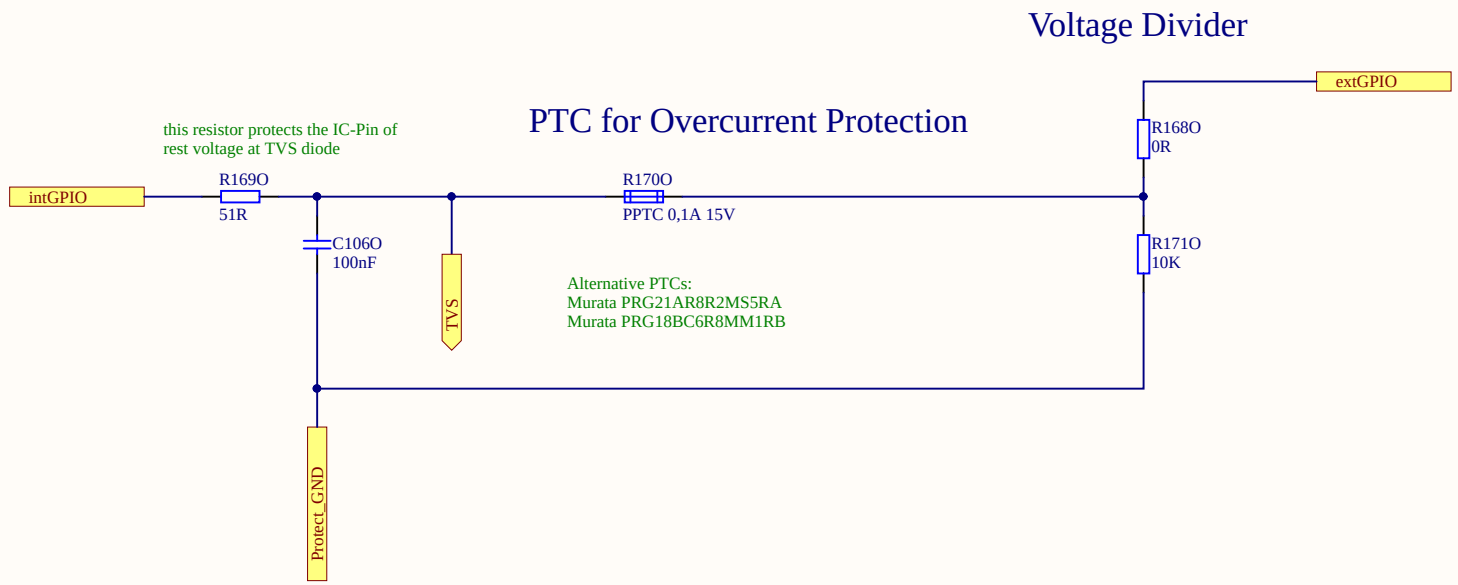
Title LevelShifting_Isolation.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	Sheet 19 of 36



Title External_IO_Protection.SchDoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
		Sheet 20 of 36	



Title External_IO_Protection.SchDoc		UltraZohm www.ultrazohm.com
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 20 of 36



Title External_IO_Protection.SchDoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
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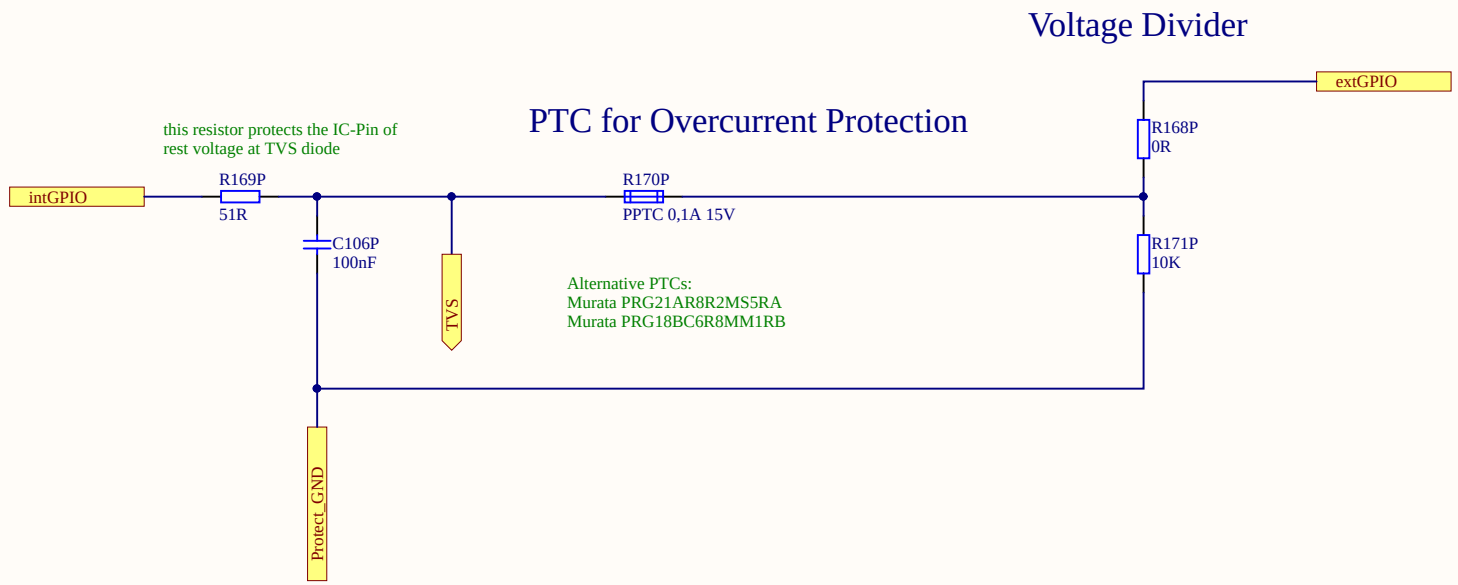

Title External_IO_Protection.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
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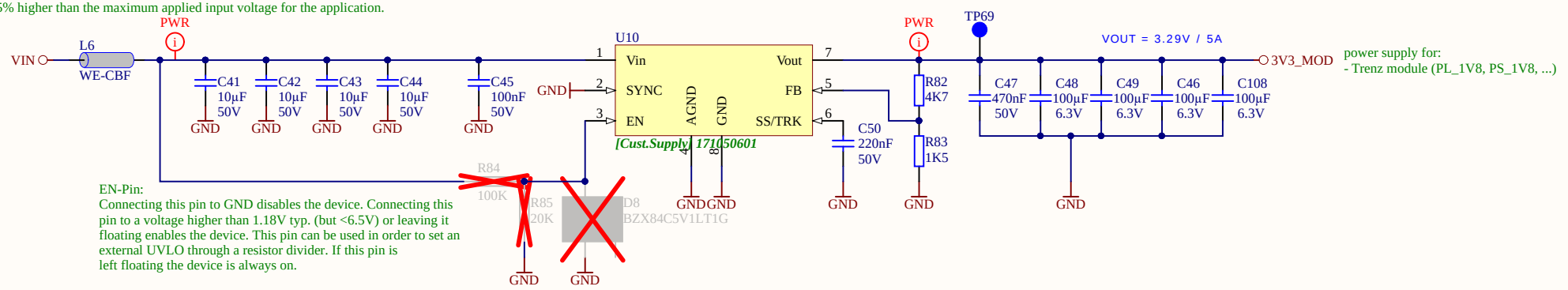
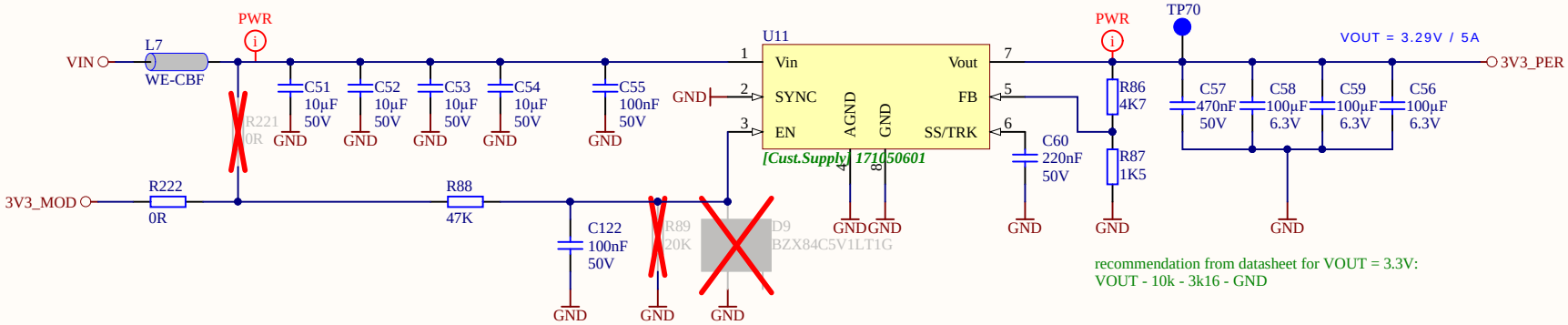
Notes: preferred to use 2x 22µF/50V capacitors at Vin, but this design uses 35V caps due to worse availability at distributors.
Datasheet: recommended minimum input capacitance is 22 µF (including derating) ceramic with voltage rating
at least 25% higher than the maximum applied input voltage for the application.



power supply for:
- Trenz module (PL_1V8, PS_1V8, ...)

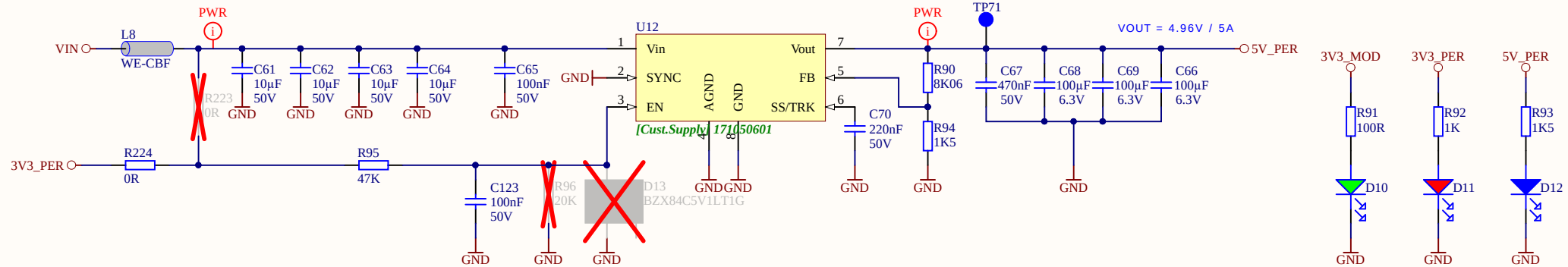
EN-Pin:
Connecting this pin to GND disables the device. Connecting this pin to a voltage higher than 1.18V typ. (but <6.5V) or leaving it floating enables the device. This pin can be used in order to set an external UVLO through a resistor divider. If this pin is left floating the device is always on.



power supply for:
- digital and analog sockets
- SD-Card
- Ethernet
- CAN

power supply for:
- digital and analog sockets

recommendation from datasheet for VOUT = 3.3V:
VOUT - 10k - 3k16 - GND



The delay time between the power supplies U10 U11 and U12 is determined by R88 C122 R95 and C123.
The delay time can be estimated as follows: t_on = -tau * ln(1-(U_en/U_max))
tau = R*C
U_en = 1,27V
U_max = output voltage of prior stage (e.g. 3V3)
Since the input current of the EN pin is about 21µA the real dealy time is a bit longer than the calculated value. With the values above there is a delay of about 5ms,

Title Power_Supply_1.SchDoc		**UltraZohm**	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
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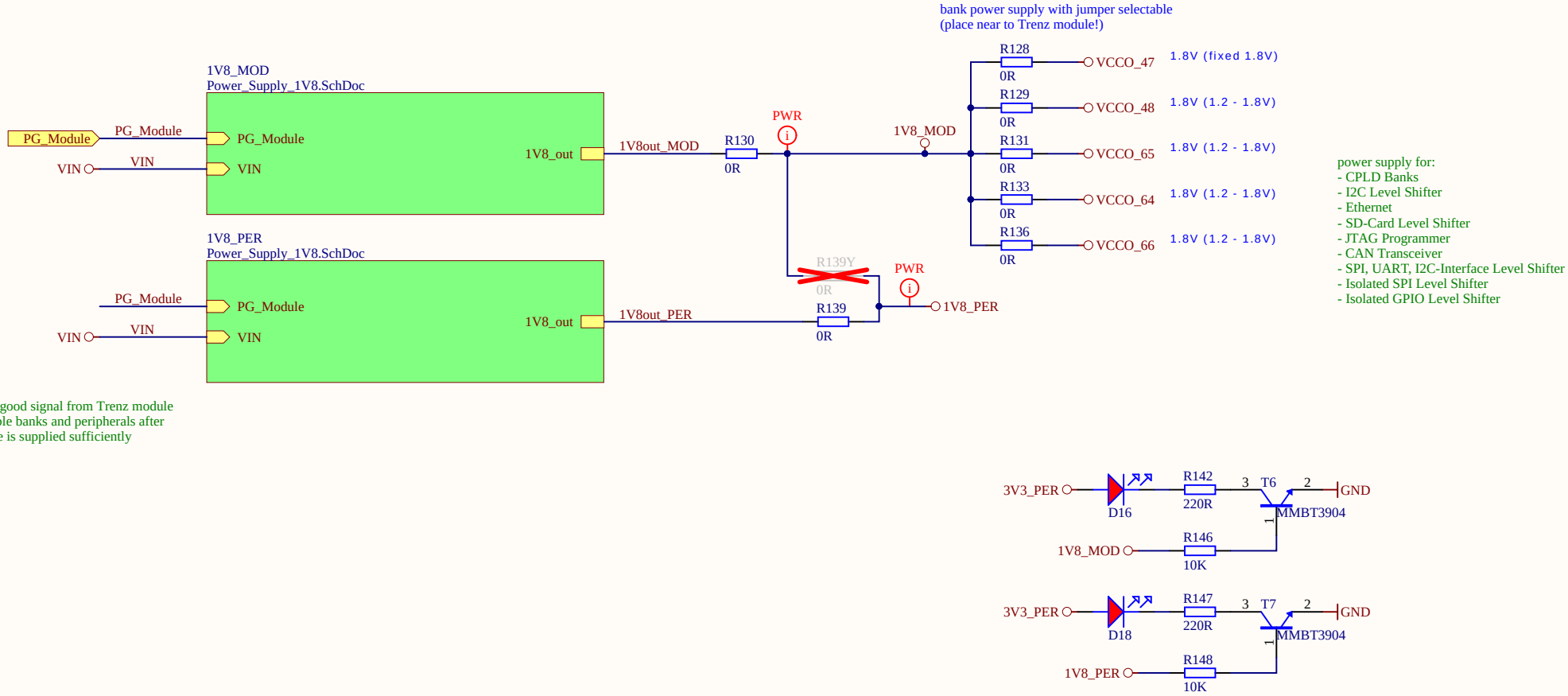
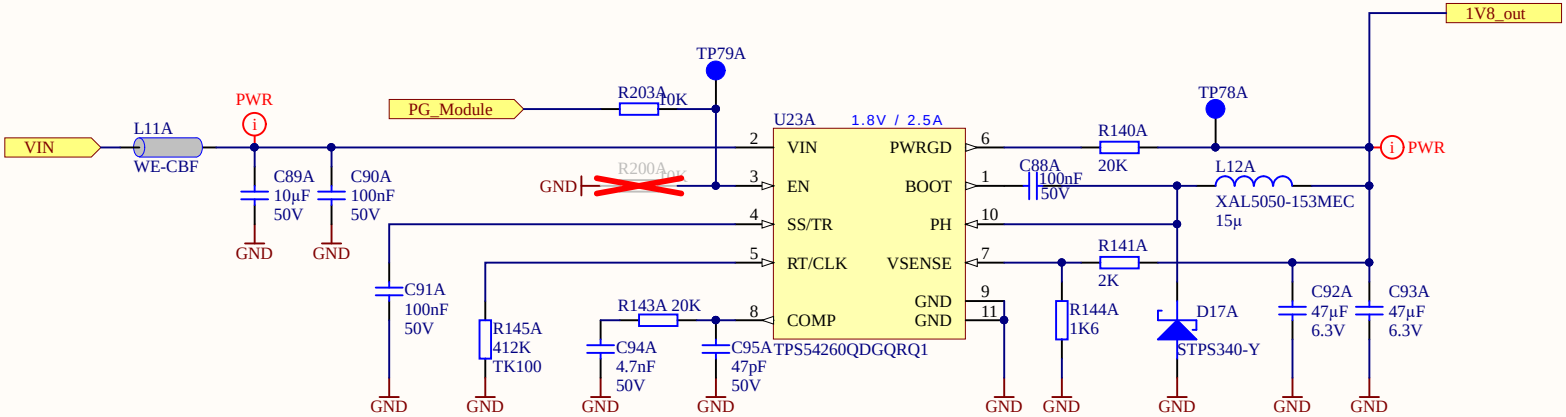
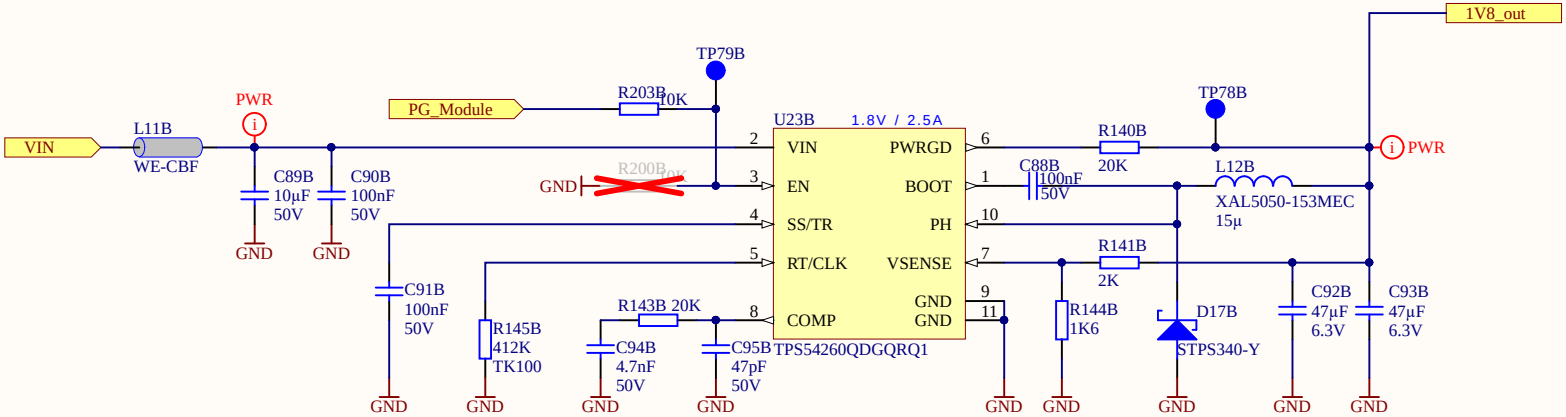


Title Power_Supply_2.SchDoc		UltraZohm www.ultrazohm.com
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021 Sheet 29 of 36



Title Power_Supply_1V8.SchDoc		UltraZohm www.ultrazohm.com
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	Date: 11.03.2021
Project: UltraZOhm_CarrierBoard.PrjPcb		Sheet 30 of 36



Title Power_Supply_1V8.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
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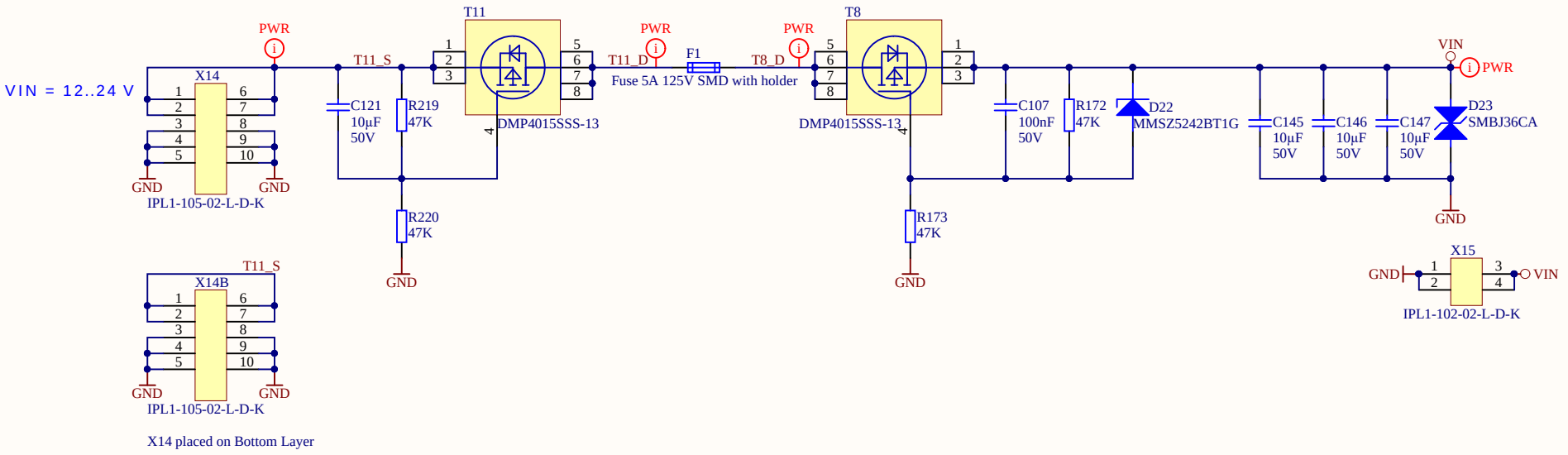
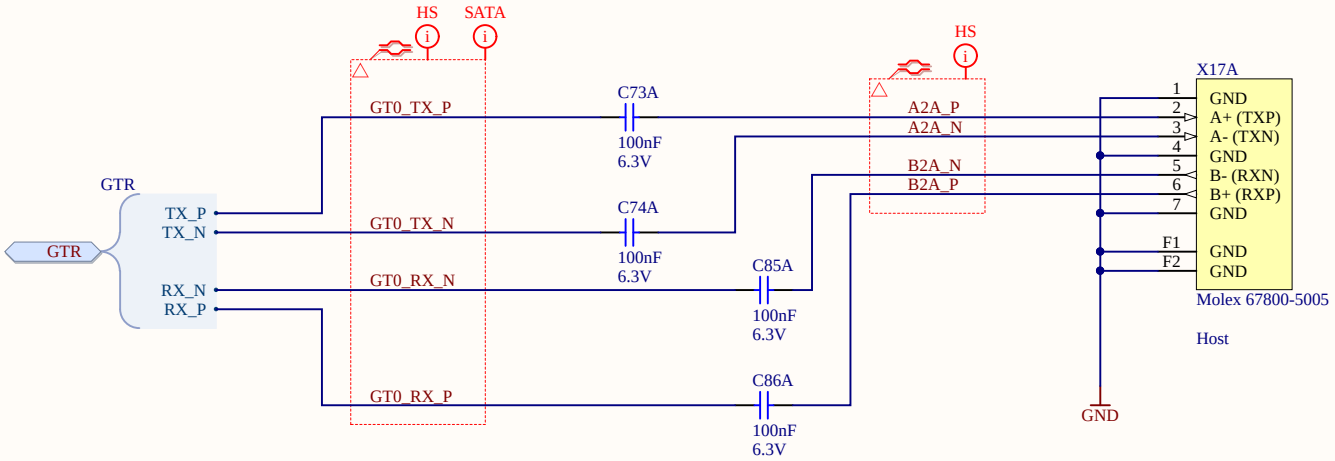


Title Power_Supply_Input.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann		
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	Sheet 27 of 36



Title GTR.schdoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
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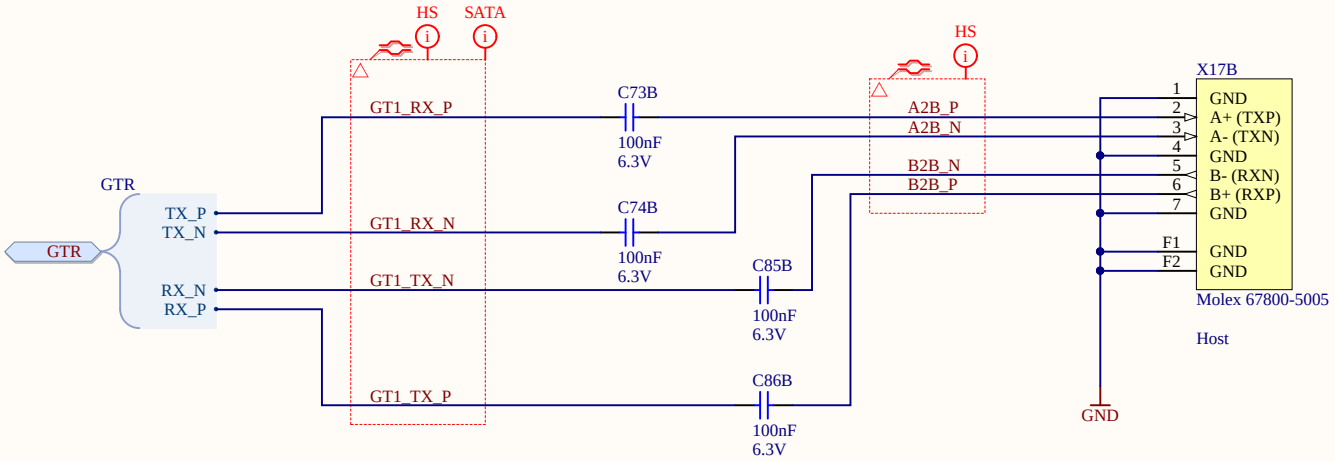

Title GTR.schdoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
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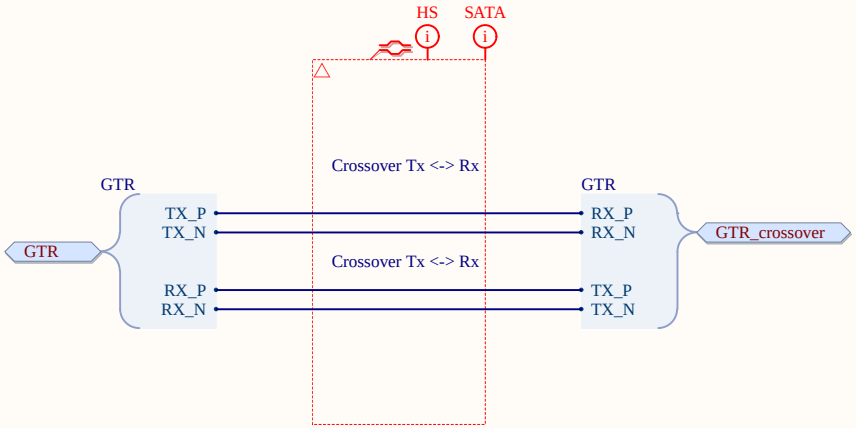

Title GTR_crossover.schdoc		UltraZohm	
Revision: 04	Design Engineer: A. Geiger & E. Liegmann	www.ultrazohm.com	
Project: UltraZOhm_CarrierBoard.PrjPcb		Date: 11.03.2021	
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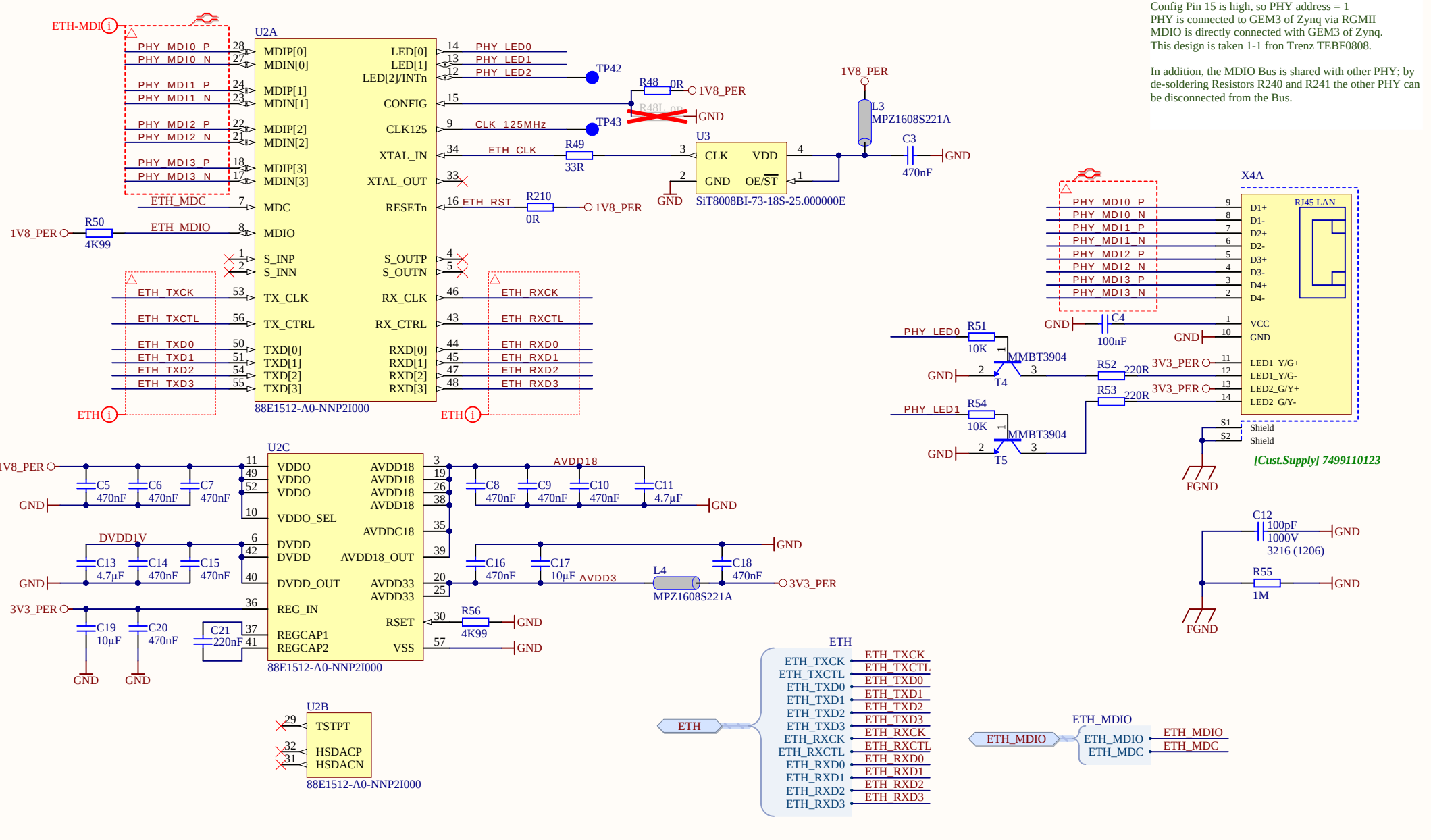
Config Pin 15 is high, so PHY address = 1
PHY is connected to GEM3 of Zynq via RGMII
MDIO is directly connected with GEM3 of Zynq.
This design is taken 1-1 fron Trenz TEBF0808.
In addition, the MDIO Bus is shared with other PHY; by de-soldering Resistors R240 and R241 the other PHY can be disconnected from the Bus.
ETH-MDI
U2A
88E1512-A0-NNP2I000
U3
SiT8008BI-73-18S-25.000000E
X4A
RJ45 LAN
U2C
88E1512-A0-NNP2I000
U2B
88E1512-A0-NNP2I000
[Cust.Supply] 7499110123
Title ETH-PHY.SchDoc
Revision: 04
Design Engineer: A. Geiger & E. Liegmann
Project: UltraZOhm_CarrierBoard.PrjPcb
UltraZohm
www.ultrazohm.com
Date: 11.03.2021
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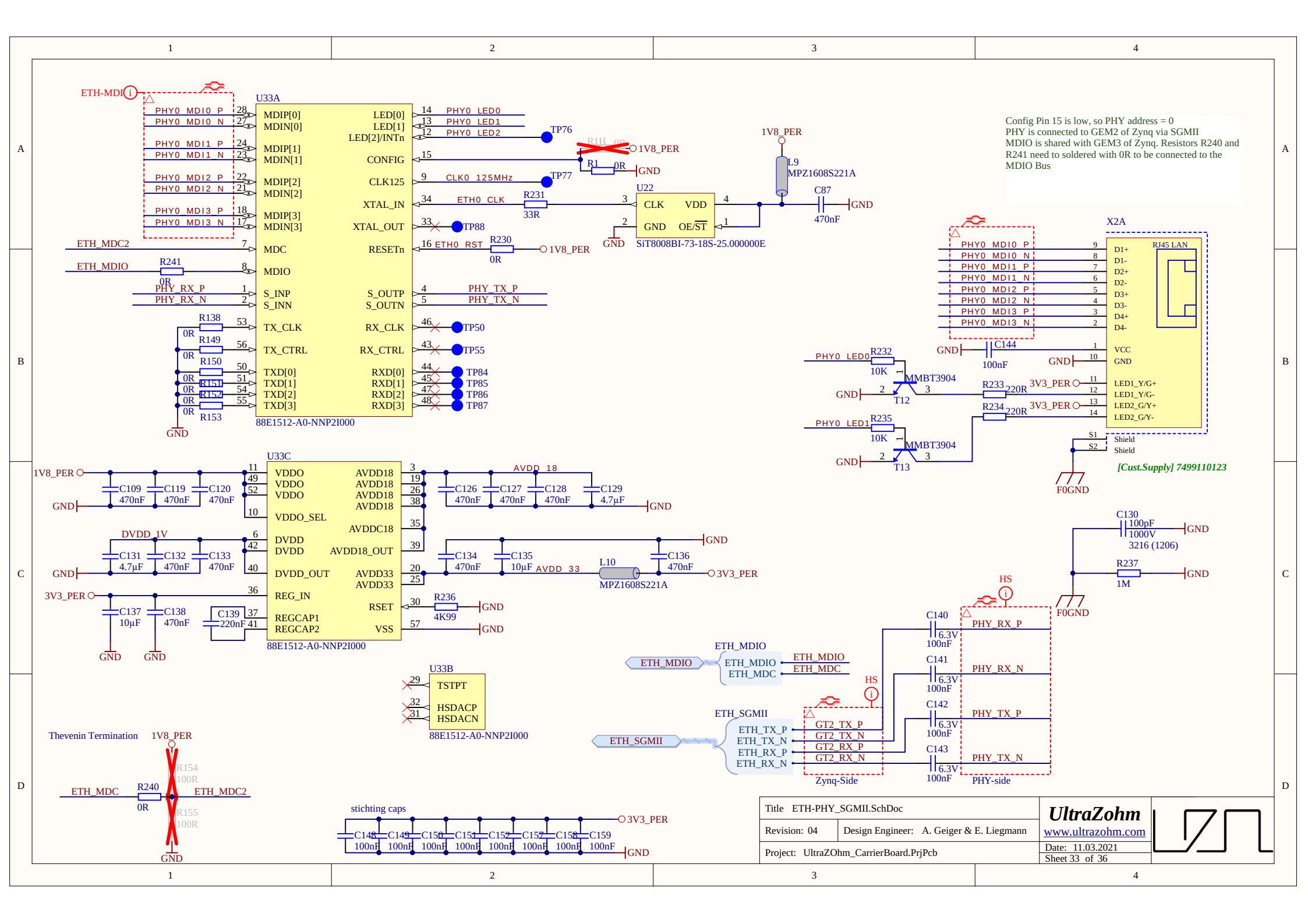
Config Pin 15 is low, so PHY address = 0
PHY is connected to GEM2 of Zynq via SGMII
MDIO is shared with GEM3 of Zynq. Resistors R240 and R241 need to soldered with 0R to be connected to the MDIO Bus
ETH-MDI
U33A
88E1512-A0-NNP2I000
U22
SiT8008BI-73-18S-25.000000E
L9
MPZ1608S221A
X2A
RJ45 LAN
U33C
88E1512-A0-NNP2I000
U33B
88E1512-A0-NNP2I000
L10
MPZ1608S221A
Thevenin Termination
stichting caps
HS
Zynq-Side
PHY-side
F0GND
[Cust.Supply] 7499110123
Title ETH-PHY_SGMII.SchDoc
Revision: 04
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Project: UltraZOhm_CarrierBoard.PrjPcb
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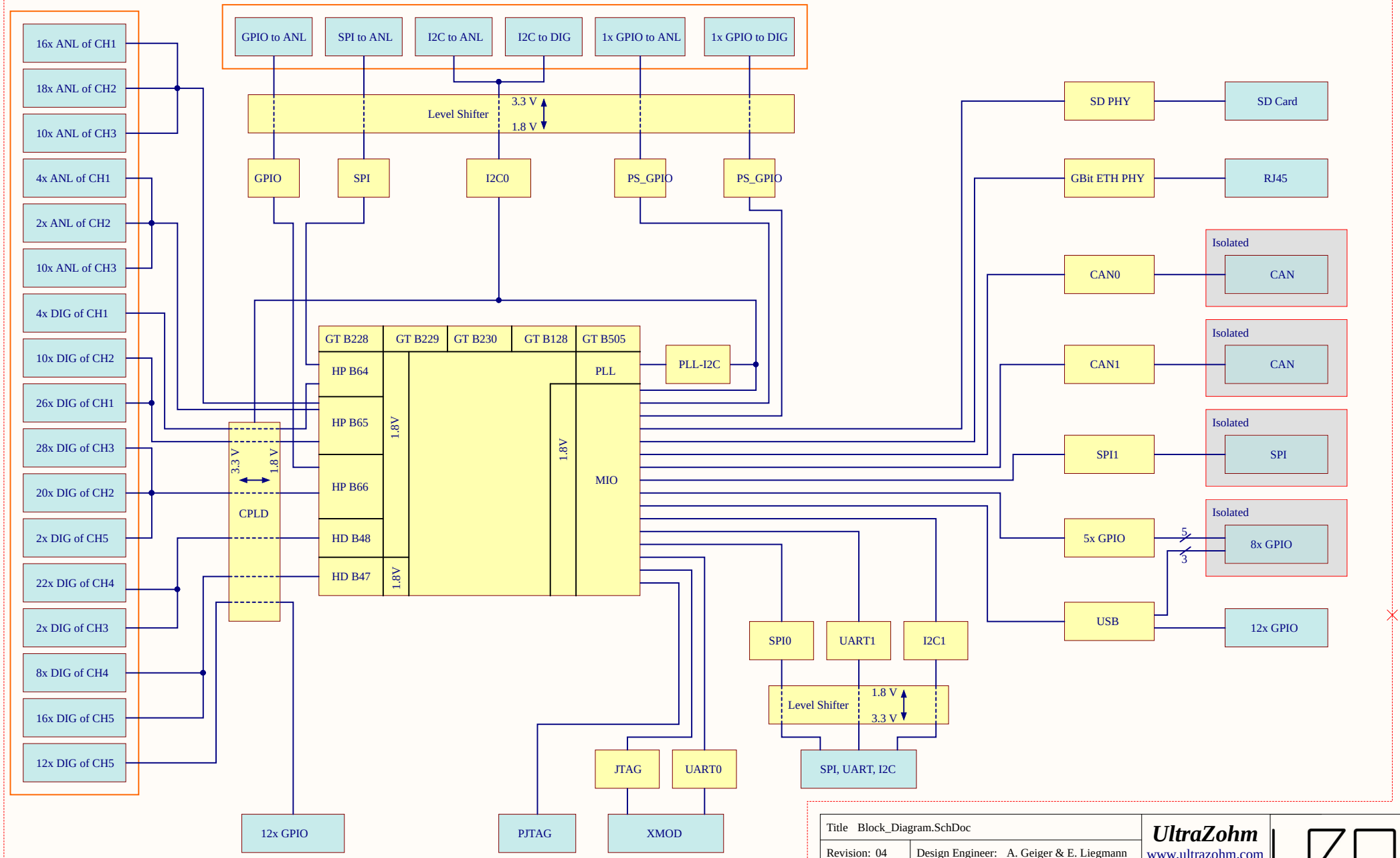

Title Block_Diagram.SchDoc		UltraZohm www.ultrazohm.com
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